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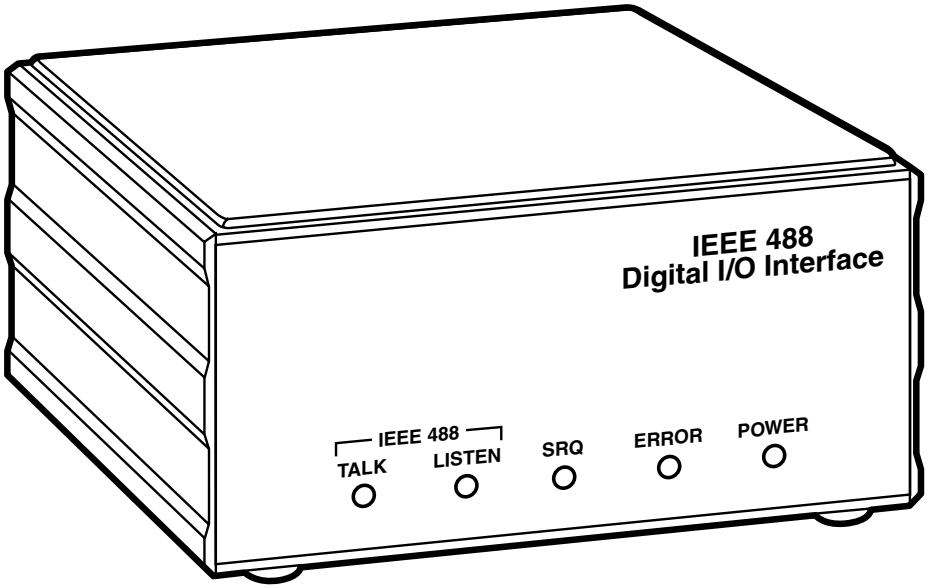
APRIL 1999
IC097A

IEEE-488/Digital I/O Interface



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NORMAS OFICIALES MEXICANAS (NOM)
ELECTRICAL SAFETY STATEMENT

INSTRUCCIONES DE SEGURIDAD

1. Todas las instrucciones de seguridad y operación deberán ser leídas antes de que el aparato eléctrico sea operado.

2. Las instrucciones de seguridad y operación deberán ser guardadas para referencia futura.

3. Todas las advertencias en el aparato eléctrico y en sus instrucciones de operación deben ser respetadas.

4. Todas las instrucciones de operación y uso deben ser seguidas.

5. El aparato eléctrico no deberá ser usado cerca del agua—por ejemplo, cerca de la tina de baño, lavabo, sótano mojado o cerca de una alberca, etc..

6. El aparato eléctrico debe ser usado únicamente con carritos o pedestales que sean recomendados por el fabricante.

7. El aparato eléctrico debe ser montado a la pared o al techo sólo como sea recomendado por el fabricante.

8. Servicio—El usuario no debe intentar dar servicio al equipo eléctrico más allá a lo descrito en las instrucciones de operación. Todo otro servicio deberá ser referido a personal de servicio calificado.

9. El aparato eléctrico debe ser situado de tal manera que su posición no interfiera su uso. La colocación del aparato eléctrico sobre una cama, sofá, alfombra o superficie similar puede bloquea la ventilación, no se debe colocar en libreros o gabinetes que impidan el flujo de aire por los orificios de ventilación.

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11. El aparato eléctrico deberá ser connectado a una fuente de poder sólo del tipo descrito en el instructivo de operación, o como se indique en el aparato.

12. Precaución debe ser tomada de tal manera que la tierra fisica y la polarización del equipo no sea eliminada.

13. Los cables de la fuente de poder deben ser guiados de tal manera que no sean pisados ni pellizcados por objetos colocados sobre o contra ellos, poniendo particular atención a los contactos y receptáculos donde salen del aparato.

14. El equipo eléctrico debe ser limpiado únicamente de acuerdo a las recomendaciones del fabricante.

15. En caso de existir, una antena externa deberá ser localizada lejos de las lineas de energia.

16. El cable de corriente deberá ser desconectado del cuando el equipo no sea usado por un largo periodo de tiempo.

17. Cuidado debe ser tomado de tal manera que objectos liquidos no sean derramados sobre la cubierta u orificios de ventilación.

18. Servicio por personal calificado deberá ser provisto cuando:

    A: El cable de poder o el contacto ha sido dañado; u

    B: Objectos han caído o líquido ha sido derramado dentro del aparato; o

    C: El aparato ha sido expuesto a la lluvia; o

    D: El aparato parece no operar normalmente o muestra un cambio en su desempeño; o

    E: El aparato ha sido tirado o su cubierta ha sido dañada.

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1. Specifications

Connectors—(1) standard IEEE-488 with metric studs, (1) DB25 female

Indicators—(5) LEDs: Talk, Listen, SRQ, Error, Power

Power—115 VAC, 60 Hz

Size—2.7"H x 5.4"W x 7.5"D (6.9 x 13.7 x 19.1 cm)

Weight—2.3 lb. (1.1 kg)

2. Introduction

2.1 Description

The IEEE-488/Digital I/O Interface is a digital input and output interface to the IEEE 488 bus. Each unit has 40 TTL-level digital I/O lines, which are divided into five eight-bit ports. With your IEEE 488 software, you can program each port as input or output.

The Digital I/O Interface has several versatile features. It asserts a trigger output signal on the Group Execute Trigger (GET) command. Edge-triggered inputs can generate a Service Request on the bus. You can program six data formats via software, including ASCII hexadecimal, ASCII character, ASCII binary, binary, high-speed binary, and ASCII decimal. The Interface also accepts individual bit set and bit clear commands. Programmable terminators facilitate interfacing to various controllers.

A status mode enables the controller to interrogate the programmed status of the Digital I/O Interface at any time. The unit initiates a self-test at power-on that checks for proper RAM and ROM operation.

When addressed to talk, the Interface will output data from all forty bits or a selected 8-bit port. When addressed to listen, the unit will input data and programming information from the controller, and output the data to the appropriate I/O port.

2.2 Abbreviations

The IEEE 488 abbreviations described in Table 1-1 are used throughout this manual.

Table 1-1. IEEE 488 Abbreviations.

Abbreviation	Meaning
addr n	IEEE bus address “n”
ATN	Attention line
CA	Controller Active
CR	Carriage Return
data	Data String
DCL	Device Clear
GET	Group Execute Trigger
GTL	Go To Local
LA	Listener Active
LAG	Listen Address Group
LF	Line Feed
LLO	Local Lock Out
MLA	My Listen Address
MTA	My Talk Address
PPC	Parallel Poll Configure
PPU	Parallel Poll Unconfigure
SC	System Controller
SDC	Selected Device Clear
SPD	Serial Poll Disable
SPE	Serial Poll Enable
SRQ	Service Request
TA	Talker Active
TAD	Talker Address
TCT	Take Control
term	Terminator
UNL	Unlisten
UNT	Untalk
*	Unasserted

3. Getting Started

3.1 What the Package Includes

Your Digital I/O Interface package should contain the following items.

- Digital I/O Interface
- Digital I/O Port Mating Connector
- Power supply
- This user's manual

Check for any obvious signs of physical damage that may have occurred during shipment. If anything is missing or damaged, please contact Black Box immediately at 724-746-5500. Retain all shipping materials in case you need to ship the product back to Black Box.

3.2 Configuration

The Digital I/O Interface has one internal 8-position DIP switch that determines the unit's IEEE address and its default IEEE-bus output terminator. Set this switch before powering on the Interface. Figure 3-1 illustrates the factory-default setting for SW1.

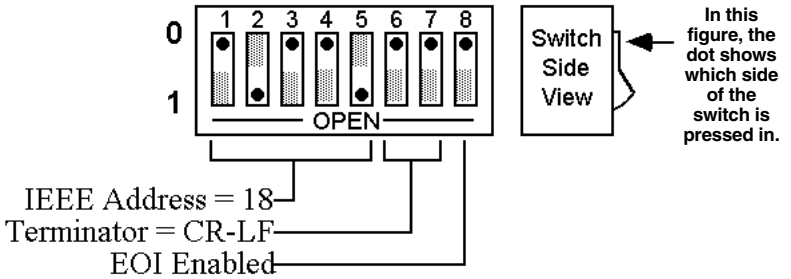


Figure 3-1. SW1 Factory Default Settings.

To modify any of these defaults, follow this simple procedure. Disconnect the power supply from the AC line and from the interface. Disconnect any IEEE or digital I/O cables before disassembly.

WARNING!

NEVER open the Digital I/O Interface case while it is connected to the AC line. You might be killed or injured, or the equipment might fail.

Remove the four screws located in each corner of the rear panel. Hold the case firmly and pull the rear panel outward, noting the slot location of the main circuit board. Modify those parameters that are appropriate for your installation and reassemble the unit. Slide the main circuit board into the previously noted slot and tighten the four screws into the rear panel.

3.2.1 IEEE 488 Address Selection

Set the IEEE 488 bus address to a value from 0 through 30 using DIP switches SW1-1 through SW1-5. The address is read *only* at power-on. You can select the address by simple binary weighting with SW1-1 as the least significant bit and SW1-5 as the most significant bit. The factory default is address 18. If you select address 31, it defaults to address 30 because the IEEE 488 standard has reserved address 31.

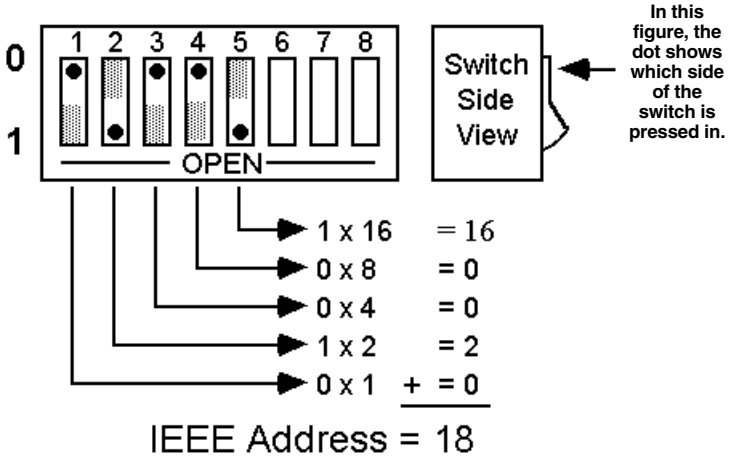


Figure 3-2. SW1: Selecting the IEEE Bus Address.

3.2.2 IEEE Bus Output Terminator Selection

DIP switches SW1-6 through SW1-8 determine the terminating characters sent on output by the Interface. The terminator switches are read only at power-on, but can be changed by the controller through the Terminator command. If power is cycled after the unit receives the Terminator command, then the unit will once again default to the switch settings. The factory default settings are Carriage Return–Line Feed with EOI asserted.

The Interface ignores all terminators *received* from the bus controller. Only the Execute (X) command is used to signal the Interface that a command string has been completed.

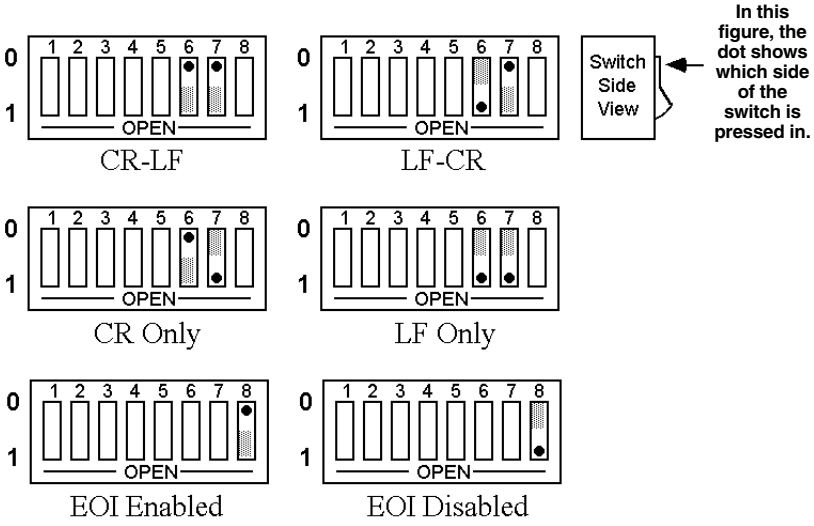


Figure 3-3. SW1 View for Selecting Terminator.

3.3 Digital Input/Output Ports

The Digital I/O Interface has 40 data lines that you can program in groups of 8 as either input or output. At power on, all 40 bits are in the input mode. Each 8-bit group is one port, beginning with Port 1 as the least significant 8 bits, and Port 5 as the most significant 8 bits.

3.3.1 Logic Levels

The data and handshake output lines will drive two TTL loads. In addition, ports 1 and 2 outputs are 5-volt CMOS compatible. All input lines are less than 1.5 TTL loads. All inputs are protected against damage caused by high static voltages. Take normal precautions to limit the input voltages to -0.3 to +7.0 volts. All I/O lines are referenced to COMMON (Pin 50).

3.3.2 Digital I/O Port Pinouts

Figure 3-3 illustrates the digital edge connector as viewed from the rear of the Interface. Table 3-1 describes the function of each pin on the connector.

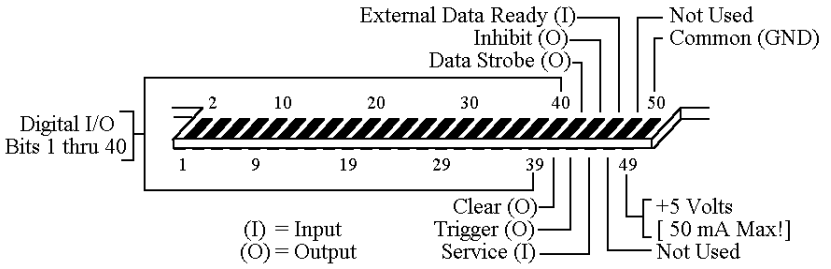


Figure 3-4. Rear Panel I/O Connector Pinout.

Table 3-1. Pin Functions on the I/O Connector.

Pin	Description
1 through 8	DATA PORT 1 (Input or Output). Pin 1 is bit 1 (LSB), Pin 8 is bit 8 (MSB). Least significant port.
9 through 16	DATA PORT 2 (Input or Output). Pin 9 is bit 1 (LSB), Pin 16 is bit 8 (MSB).
17 through 24	DATA PORT 3 (Input or Output). Pin 17 is bit 1 (LSB), Pin 24 is bit 8 (MSB).
25 through 32	DATA PORT 4 (Input or Output). Pin 25 is bit 1 (LSB), Pin 32 is bit 8 (MSB).
33 through 40	DATA PORT 5 (Input or Output). Pin 33 is bit 1 (LSB), Pin 40 is bit 8 (MSB). Most significant port.
41	CLEAR (Output)
42	DATA STROBE (Output)
43	TRIGGER (Output)
44	INHIBIT (Output)
45	SERVICE INPUT (Input)
46	EXTERNAL DATA READY (EDR) (Input)
47, 48	Not used.
49	+5 Volts (DO NOT EXCEED 50-MA LOAD!)
50	I/O COMMON (Ground)

3.3.3 Control Lines

Five control lines enable handshaking of digital I/O data transfer to the Digital I/O Interface. They are automatically activated with the corresponding I/O activity and can also be independently activated with the Handshake (Hn) command.

Clear (Pin 41)

The Clear output is pulsed for approximately 50 microseconds after a Device Clear (DCL), Selected Device Clear (SDC), or Interface Clear (IFC) command has been sent on the bus. The Clear line is normally active high. The Invert command (I8) will program it active low. The Handshake command (H0) can pulse the Clear line, independently of any I/O operations.

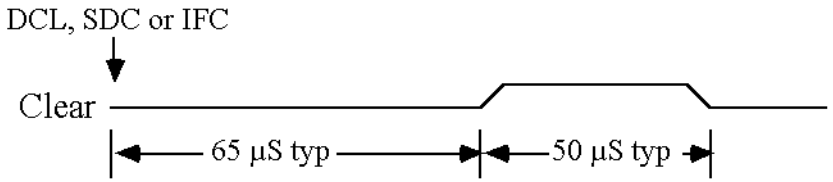


Figure 3-5. Timing Diagram for Clear Output.

Data Strobe (Pin 42)

The Data Strobe output is pulsed for approximately 50 microseconds after new data is output on the I/O port. The Data Strobe line is normally active high, but may be programmed active low by the Invert command (I4). The Handshake command (H1) can pulse the Data Strobe line, independently of any I/O operations.

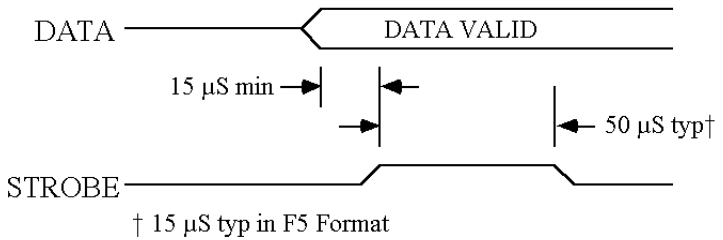


Figure 3-6. Timing Diagram for Strobe Output.

External Data Ready (EDR) (Pin 46)

The External Data Ready (EDR) line is an edge sensitive input that is used to latch input data. It is used in conjunction with the Data Ready command (R1). The EDR signal must be at least one microsecond wide and must have a rise and fall time of less than one microsecond. The EDR line is normally rising-edge sensitive, but can be programmed with the Invert command (I32) to be falling-edge sensitive. See Figure 3-6 for timing relationships.

When using the EDR line with the R1 command, data is not read when the Digital I/O Interface is addressed to talk as with R0. The Interface will only output data when the EDR line transitions.

EDR will not function in the high-speed binary (F5) format.

Inhibit (Pin 44)

The Inhibit output is asserted while data on the selected I/O port is being read into the I/O port buffer. This line is normally active high, but may be programmed active low by the Invert command (I1). You can program the Inhibit line independently of any I/O operations with the Inhibit command (Qn). See Figure 3-6 for timing relationships.

The Inhibit line is asserted once for each data read operation for all format (Fn) modes except high-speed binary (F5). In this mode, it is asserted for the first data read after the Interface is addressed to talk. On the last data-byte transfer, the data is read again with Inhibit asserted in anticipation of another data transfer. If you use Inhibit to sequence external hardware, be aware that this line will pulse N+1 times, where N is the number of total (5-byte) data transfers.

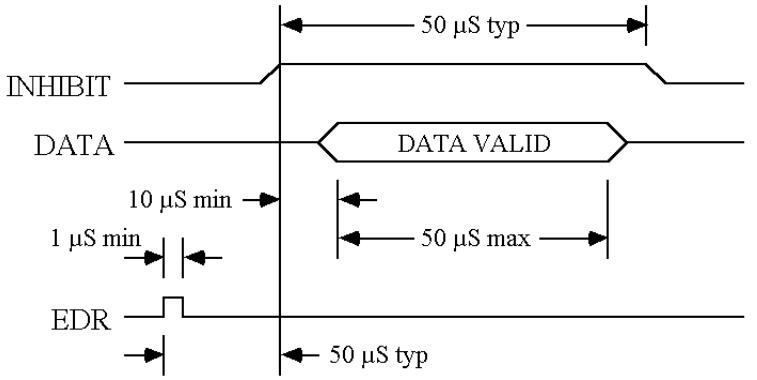


Figure 3-7. Timing Diagram for EDR Input and Inhibit Output.

Trigger (pin 43)

The Trigger output pulses for approximately 50 microseconds after a GET (Group Execute Trigger) command is received from the bus controller. The trigger pulse is normally active high, but can be made active low with the Invert command (I2). The Handshake command (H2) can pulse the Trigger line, independently of any bus activity.

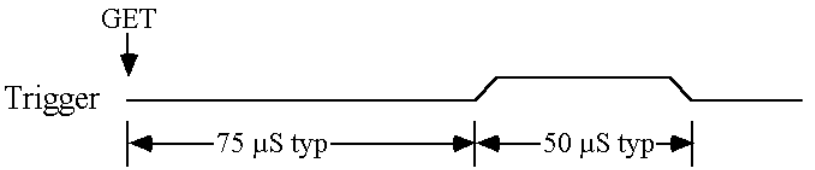


Figure 3-8. Timing Diagram for Trigger Output.

Service (Pin 45)

The Service input is an edge-sensitive input that can generate a bus Service Request (SRQ). It's enabled with the SRQ command (M1) and defaults to rising-edge sensitive. You can use the Invert command (I64) to program it to be falling-edge sensitive.

3.4 Implementing the IEEE 488 Bus

The Digital I/O Interface implements many of the capabilities defined by the IEEE 488 1978 specification. However, it does not support or respond to these bus single-line and multi-line commands.

- Remote Enable (REN)
- Go to Local (GTL)
- Local Lockout (LLO)
- Take Control (TCT)
- Parallel Poll (PP)
- Parallel Poll Configure (PPC)
- Parallel Poll Unconfigure (PPU)
- Parallel Poll Disable (PPD)

3.4.1 My Talk Address (MTA)

When the Digital I/O Interface is addressed to talk (R0) it asserts Inhibit, reads the data from all ports, un-asserts Inhibit, and outputs the data to the bus in the format as defined by the Fn, Pn, and Gn commands. The output-bus terminators are appended to the output with the exception of the F4 and F5 formats. F4 does not append terminators. The output format of F5 will be described separately. After output in the F0 through F4 formats, you must re-address the Digital I/O Interface to talk to perform subsequent reads.

In the RI mode, it will wait for the selected EDR transition before reading the data and formatting it for output. If the EDR line has transitioned before being addressed to talk, the data read at the time of EDR will be buffered for output when next addressed to talk. If EDR transitions again before the previous EDR buffered data has been output, the Interface will generate an EDR Overrun error and ignore the EDR read request. After output in the F0 through F4 formats, the Digital I/O Interface must be re-addressed to talk to perform subsequent buffered output of EDR captured data.

In either Rn mode, the Digital I/O Interface can send requested status (Un) without affecting the data ports or Inhibit. After the requested status is output, the presently programmed Rn mode returns.

EDR cannot be used to capture data in the high-speed binary format (F5). When addressed to talk in this format, the Interface asserts Inhibit and outputs the binary data to the bus with EOI asserted on the fifth byte. When the last data byte is transferred, the data is read again in anticipation of another data transfer. If Inhibit is used to sequence external hardware, this line will pulse N+1 times, where N is the number of total (5 byte) data transfers. In this format, the Digital I/O Interface does not have to be re-addressed to talk to read the ports multiple times.

With all Fn formats, the data is output in the sequence PORT5, PORT4, PORT3, PORT2, PORT1.

3.4.2 My Listen Address

When the Interface is addressed to listen in the F0 through F4 format, it accepts characters from the active talker and interprets these characters as commands and command parameters. These commands are explained in **Chapter 4**.

In the high speed binary format (F5), the command interpreter is disabled. The Digital I/O Interface treats all bytes received as data to be output to the Digital I/O ports. Each time it receives five bytes *or* detects EOI, it pulses the Data Strobe for approximately 15 microseconds. Data is expected in the sequence PORT5, PORT4, PORT3, PORT2, PORT1.

If only two bytes are received, with EOI asserted on the second byte, the Interface will update PORT5 with the first byte received and PORT4 with the second, and pulse the Data Strobe. Since the interface treats all received characters as data, the Status (Un) command will not be recognized.

3.4.3 Device Clear (DCL and SDC)

In the F0 through F4 formats, Device Clear resets the Interface to power-on defaults and pulses the Clear output line for approximately 50 microseconds.

In the high speed binary format (F5), it enables the command interpreter and changes the format to F0. All other parameters remain unchanged. In addition, the Clear output line is *not* pulsed by DCL or SDC when the interface is in F5. This is the only programmable method to exit the F5 format.

3.4.4 Group Execute Trigger (GET)

When the Interface recognizes a GET, it pulses the Trigger output line for approximately 50 microseconds.

3.4.5 Interface Clear (IFC)

IFC places the Interface in the Talker/Listener Idle State and pulses the Clear output line for approximately 50 microseconds.

3.4.6 Serial Poll Enable (SPE)

When Serial Poll is enabled, the Digital I/O Interface sets itself to respond to a serial poll with its serial-poll status byte if addressed to talk. When the serial-poll byte is accepted by the controller, any pending SRQs are cleared. The Interface will continue to try to output its serial-poll response until it is disabled by the controller.

3.4.7 Serial Poll Disable (SPD)

Disables the Digital I/O Interface from responding to serial polls by the controller.

3.4.8 Unlisten (UNL)

UNL places the Interface in the Listener Idle State.

3.4.9 Untalk (UNT)

UNT places the Interface in the Talker Idle State.

3.5 Installation

To begin operating the Digital I/O Interface, plug the external power supply into the rear jack on the interface.

CAUTION

NEVER connect the power supply to the interface while it is connected to AC line power. If you don't observe this caution, the Digital I/O Interface could be damaged.

WARNING!

The power supply provided with the interface is for INDOOR USE ONLY. If you don't observe this warning, you might be killed or injured, or the equipment might fail.

After connecting the power supply to the interface, press the rear-panel power switch to power on the unit. All the front-panel LEDs should light for approximately one second while the Interface performs an internal ROM and RAM self-check. At the end of this self-check, all indicators should turn off except POWER.

If you obtain the above response, then your Interface is alive and well. If all LEDs remain on, then a ROM error has occurred. If all LEDs continue to flash (except the Power LED), then a RAM error has occurred. Try cycling the power to the Interface to see if the error repeats.

If the LEDs do not flash and the POWER indicator does not remain lit, there may not be any power supplied to the interface. Check to make sure that AC power is supplied to the power supply, and that the supply is properly connected to the unit. If the problem is unresolved, call for technical support.

4. Command Descriptions

4.1 Introduction

Control of the Digital I/O Interface is implemented with 17 bus commands, described here in detail. Examples are given for many of the commands using a Hewlett-Packard XS computer in the immediate mode. Each command is terminated by the "END LINE" key on the HP-85 in order to execute the command. Set the Interface's bus address to 18 for all examples.

NOTE

The EXECUTE command (X) must follow all command strings sent to the Digital I/O Interface. No commands are executed until the unit receives an X.

4.2 Bit Set (An)

The Bit Set command programs a logical one output to a bit described by the argument "n." Setting a bit may represent either a +5-volt or 0-volt output, depending on whether an Invert command (116) has been sent. If data is active high (default condition), then Bit Set outputs +5 volts. If you wish to set multiple bits within the same command string, you must include an Execute command (X) after every Bit Set command.

You must configure the bit you wish to set as an output bit by the Configure command to be valid. The Strobe output line is not pulsed when the Bit Set command is sent.

An Bit n (1 through 40) is set to logic one

Example:

```
CLEAR 7 18                  reset the Digital I/O Interface
OUTPUT 718;"C5X"            configure all ports as output
OUTPUT 718;"A22X"           set bit 22 to a logic one
OUTPUT 718;"A23XA24X"       set bits 23 and 24 to a logic one
```

4.2 Bit Clear (Bn)

The Bit Clear command will clear to a logic zero an output bit described by the argument "n." Clearing a bit may represent either a 0 volt or +5 volt output,

depending on whether an Invert command (116) has been sent. If data is active high (default condition), then Bit Clear outputs 0 volts. When multiple Bit Clear commands are used in the same command string, an Execute command (X) must follow each command.

The bit that is being cleared must have been defined as an output by the Configure command in order to be valid. The Strobe output line is not pulsed when the Bit Clear command is sent.

Bn Bit n (1 through 40) is cleared to a logic O

Example:

```
CLEAR 718                  reset the Digital I/O Interface
OUTPUT 718;"CSX"           configure all ports as output
OUTPUT 718;"A7XA8XA9X"     set bits 7, 8, and 9 to +5 volts
OUTPUT 718;"B7X"           clear bit 7 to zero volts
OUTPUT 718;"B8XB9X"        clear bits 8 and 9 to zero volts
```

4.4 Bus Input/Output (Gn)

The Bus Output command determines whether input port data, output port data or both will be transmitted on the bus when the Digital I/O Interface is addressed to talk. The amount of data sent depends on the Pn command.

The G0 default mode causes all input and output port data to be sent to the controller when addressed to talk. The G1 mode causes only data from the ports programmed as inputs to be returned when addressed to talk. The G2 mode causes only data from ports programmed as outputs to be returned when addressed to talk.

If all ports are programmed as outputs with G1 selected and the Interface is addressed to talk, nothing will be transmitted and the bus will hang. The converse will also cause the bus to hang with all ports programmed as inputs and G2 selected.

G0 *Input* and *output* port data is sent on talk.
G1 Only *input* port data is sent on talk.
G2 Only *output* port data is sent on talk.

Example:

```
CLEAR 718              reset the Digital I/O Interface
OUTPUT 718;"P0ClX"     port 1 as output, ports 2-5 as input
OUTPUT 718;"GlX"       select only input ports
ENTER 718;A$           read data from the input ports
DISP A$                display shows FFFFFFFF (data depends on what is
                       connected)
OUTPUT 718;"G2X"       select output ports
ENTER 718;A$           read data from the output ports
DISP A$                display shows 00 (outputs default to 0)
```

4.5 Configure (Cn)

Ports 1 through 5 are configured as inputs or outputs with the Configure command. Each port is eight bits wide. At power-on, all ports are initialized as inputs. The Configure command is usually the first command to be sent after power on. All ports programmed as outputs will be set to a logic zero after receiving the Configure command. The actual output level is dependent on the Invert command (116).

Cn Mode n (0 through 5) defines which ports are input and output

Port	5	4	3	2	1
C0	in	in	in	in	in
C1	in	in	in	in	out
C2	in	in	in	out	out
C3	in	in	out	out	out
C4	in	out	out	out	out
C5	out	out	out	out	out

in=programmed as an input port
out=programmed as an output port

Example:

```
CLEAR 718              reset the Digital I/O Interface
OUTPUT 718;"ClX"       select port 1 as output, ports 2 through 5 as inputs
```

4.6 Data (Dn...Z)

The Data command outputs up to 40 bits of data to the output ports. The number of bits that can be sent with the Data command is limited by the number of bits programmed as outputs. For formats F0 through F3, if the amount of data sent is less than the the number of bits programmed as outputs, the least-significant bits will contain the data sent and the most-significant bits will be cleared to logic zero. If a single port is selected with the Port command, only eight bits may sent with the Data command. The Data Strobe output is pulsed for approximately 50 microseconds after new data is output on the selected ports.

For formats F0 through F3, data sent by the controller is contained within a prefix (D) and a suffix (Z). In format F4, the five bytes immediately following the prefix (D) is interpreted as data and the suffix (Z) is not used. For the high-speed binary F5 format, all bytes received are treated as data and the prefix and suffix are not used. Refer to the Fn command for additional details.

Dn...Z **n...** represents the data to be output, terminated by **Z**.

NOTE

In the F4 mode, the Z terminator is not allowed.

Example:

```
CLEAR 718                    reset the Digital I/O Interface
OUTPUT 718;"C5P1X"           all ports as output, select port 1
OUTPUT 718;"D55ZX"           send 55 to port 1
ENTER 718;A$                 read data from port 1
DISP A$                      display shows 55

OUTPUT 718;"P0X"             select all ports
OUTPUT 718;"D1234567890ZX"   send data to all 40 bits
ENTER 718;A$ DISP A$         read data from the Digital I/O Interface
DISP A$                      display shows 1234567890


OUTPUT 718;"D123ZX"          send 12 bits of data to the least
ENTER 718; A$                significant bits read data from
DISP A$                      the Digital I/O Interface
                             display shows 0000000123
```

```
OUTPUT 718;"P5D21ZX"        set port 5 only select all ports
OUTPUT 718;"P0X"            read data from the Digital I/O Interface
ENTER 718;A$                display shows 2100000123
DISP A$
```

4.7 Data Ready (Rn)

The Data Ready command enables digital input data to be latched. When used in conjunction with the Service Request (M2) command, the External Data Ready line can both latch the input data and signal the controller that new data is available.

In the default mode (R0) data is read when the Digital I/O Interface is addressed to talk. In the R1 mode, it will wait for the selected External Data Ready (EDR) transition before reading the data and formatting it for output. If the Digital I/O Interface is addressed to talk before EDR is asserted, the bus will hang up until the EDR pulse occurs. Once EDR is asserted, the data will remain latched until the interface is addressed to talk and the data is read by the controller. If EDR transitions again before the previous EDR buffered data has been output, the Digital I/O Interface will generate an EDR Overrun error and ignore the EDR read request.

After output in the F0 through F4 formats, the Digital I/O Interface must be readdressed to talk to perform subsequent buffered output of EDR captured data EDR cannot be used to capture data in the F5 high-speed binary format.

The EDR signal must be at least 1 microsecond wide and should have a rise and fall time of less than 1.0 microsecond. The EDR line defaults to rising-edge sensitive, but can be changed to falling-edge sensitive with the Invert command (132).

R0 Data is not latched, and is read whenever the Digital I/O Interface is addressed to talk.
R1 Data is latched on an EDR transition.

Example:

```
CLEAR 718              reset the Digital I/O Interface
OUTPUT 718;"R1X"       data is only read after a rising-edge signal is applied
                       to the EDR line
```

4.8 End or Identify (Kn)

The (EOI) line is one of five interface management lines on the IEEE I/O Interface Bus. It is used by a talker to indicate the end of a multiple byte transfer sequence. At power-on, the setting of Switch S1 determines the default EOI mode. The controller can change the EOI mode by programming the Digital I/O Interface from the bus. In the K0 mode, the EOI line is asserted by the Digital I/O Interface on the last byte of every bus output string. In the K1 mode the EOI function is disabled (except when using the binary modes [F4 and F5]).

K0 EOI enabled, assert EOI on last byte transferred
K1 EOI disabled, do not assert EOI on last byte transferred

Example:

```
OUTPUT 718;"K1X"
```
disables EOI on last byte

4.9 Execute (X)

Commands sent to the Digital I/O Interface will result in no action until the unit is instructed to execute these commands. This is done by sending an X, usually as the last character of a command string. Commands sent without an X are stored in the internal buffer until an X is received. Any number of Execute commands may be inserted into the same command string. Certain commands, such as Bit Set, require an X after each command in a string if more than one of that command is within the same string.

Example:

`CLEAR 718`	reset the Digital I/O Interface
`OUTPUT 718;"F2"`	send “F2” to the Digital I/O Interface command input buffer
`OUTPUT 718;"X"`	instruct the Digital I/O Interface to execute its command input buffer
`OUTPUT 718;"A1XA2X"`	two Bit Set (A) commands are within the same string, requiring an X after each command.

4.10 Format (Fn)

The Format command determines the method by which input and output data will be described. Six data formats are available.

F0 ASCII Hexadecimal (4 bits per character)
Fl ASCII Character (4 bits per character)
F2 ASCII Binary (1 bit per character)
F3 ASCII Decimal (8 bits per number)
F4 Binary (each byte represents 8 bits)
F5 High Speed Binary (each byte represents 8 bits)

F0 Format—ASCII Hexadecimal

In the default F0 format, the data is described in ASCII hexadecimal, with each character having a value from 0 thru 9 or A through F. Each ASCII character describes 4 bits of data.

F0 Character	Decimal Equiv	F0 Character	Decimal Equiv
0	0	8	8
1	1	9	9
2	2	A	10
3	3	B	11
4	4	C	12
5	5	D	13
6	6	E	14
7	7	F	15

Data received for output to the digital ports must be contained within a prefix (D) and a suffix (Z). If the amount of data sent is less than the number of bits programmed as outputs, the least-significant bits will contain the data sent and the most-significant bits will be cleared to logic zero. If the data sent is greater than the number of bits programmed for output or selected by the Pn command, the Digital I/O Interface will generate a conflict error and ignore the entire command string. The Data Strobe output is pulse for approximately 50 microseconds after new data is output on the selected port(s).

When the Digital I/O Interface is addressed to talk (R0) it asserts Inhibit, reads the data from all ports, unasserts Inhibit and outputs the number of characters determined by the Gn and Pn commands. Leading zeros are not suppressed and the bus terminators are appended to the output. After output the Interface must

be re-addressed to talk to perform subsequent reads. EDR (Rl) may also be used to capture data in this format.

Example:

```
DIM A$[50]              dimension the length of A$
CLEAR 718               reset the Digital I/O Interface
OUTPUT 718;"C2G2X"      configure ports 1 & 2 as output
OUTPUT 718;"D4E6BZX"    output hexadecimal 4E6B to ports 1 & 2
ENTER 718;A$            read data from the Digital I/O Interface
DISP A$                 display shows 4E6B
```

F1 Format—ASCII Character

In the F1 format, the data is coded and transmitted in ASCII Characters with the four least significant bits of each ASCII character representing four bits of data.

F1 Character	Decimal Equiv	F1 Character	Decimal Equiv
0	0	8	8
1	1	9	9
2	2	:	10
3	3	;	11
4	4	<	12
5	5	=	13
6	6	>	14
7	7	?	15

Data received for output to the digital ports must be contained within a prefix (D) and a suffix (Z). If the amount of data sent is less than the number of bits programmed as outputs, the least significant bits will contain the data sent and the most significant bits will be cleared to logic zero. If the data sent is greater than the number of bits programmed for output or selected by the Pn command, the Digital I/O Interface will generate a conflict error and ignore the entire command string.

The Data Strobe output is pulsed for approximately 50 microseconds after new data is output on the selected port(s).

When the Digital I/O Interface is addressed to talk (R0), it asserts Inhibit, reads the data from *all* ports, unasserts Inhibit, and outputs the number of characters determined by the Gn and Pn commands. Leading zeros are not suppressed and

the bus terminators are appended to the output. After output the Digital I/O Interface must be re-addressed to talk to perform subsequent reads. EDR (R1) may also be used to capture data in this format.

Example:

```
OUTPUT 718;"F1X"          select ASCII Character format
ENTER 718; A$             read data from the Digital I/O Interface
DISP A$                   display shows 4>6;
OUTPUT 718;"D1??2ZX"      send 1??2 to the Digital I/O Interface
ENTER 718;A$              read data from the Digital I/O Interface
DISP A$                   display shows 1??2
```

F2 Format—ASCII Binary

In the F2 format, each data bit is described with an ASCII 0 or 1. Each byte is formatted in two 4-bit multiples separated by semicolons.

F2 String	Decimal Equiv	F2 String	Decimal Equiv
0000;0000	0	0000;1001	9
0000;0001	1	0000;1010	10
0000;0010	2	0000;1011	11
0000;0011	3	0000;1100	12
0000;0100	4	0000;1101	13
0000;0101	5	0000;1110	14
0000;0110	6	0000;1111	15
0000;0111	7	1000;0001	129
0000;1000	8	1111;1111	255

Data received for output to the digital ports must be contained within a prefix (D) and a suffix (Z) and each 4-bit quantity must be separated by semicolons. Leading zeros are not required. If the amount of data sent is less than the number of bits programmed as outputs, the least significant bits will contain the data sent and the most significant bits will be cleared to logic zero. If the data sent is greater than the number of bits programmed for output or selected by the Pn command, the Digital I/O Interface will generate a conflict error and ignore the entire command string. The Data Strobe output is pulsed for approximately 50 microseconds after new data is output on the selected port(s).

When the Digital I/O Interface is addressed to talk (R0) it asserts Inhibit, reads the data from all ports, unasserts Inhibit, and outputs the number of characters determined by the Gn and Pn commands. Leading zeros are not suppressed, and the bus terminators are appended to the output. After output, the Digital I/O Interface must be re-addressed to talk to perform subsequent reads. EDR (R1) may also be used to capture data in this format.

Example:

```
OUTPUT 718;"F2X"              select ASCII/binary mode
ENTER 718;A$                  read data from the Digital I/O Interface
DISP A$                       display shows 0001;1111;1111;0001
OUTPUT 718;D100;200ZX
ENTER 718; A$                 read data from the Digital I/O Interface
DISP A$                       display shows 1111;0000;1010;0101
```

F3 Format—ASCII Decimal

In the F3 format, the data is described in decimal 8-bit multiples and transmitted in ASCII. Each decimal number (0 to 255) to be output must be separated by semicolons.

F3 Number	Decimal Equiv	F3 Number	Decimal Equiv
000	0	008	8
001	1	009	9
002	2	010	10
003	3	020	20
004	4	100	100
005	5	200	200
006	6	210	210
007	7	255	255

Data received for output to the digital ports must be contained within a prefix (D) and a suffix (Z). If the amount of data sent is less than the number of bits programmed as outputs, the least significant bits will contain the data sent and the most significant bits will be cleared to logic zero. If the data sent is greater than the number of bits programmed for output or selected by the Pn command, the Digital I/O Interface will generate a conflict error and ignore the entire command string. The Data Strobe output is pulsed for approximately 50 microseconds after new data is output on the selected port(s).

When the Digital I/O Interface is addressed to talk (R0) it asserts Inhibit, reads the data from *all* ports, unasserts Inhibit, and outputs the number of characters determined by the Gn and Pn commands. Leading zeros are not suppressed and the bus terminators are appended to the output. After output the Digital I/O Interface must be re-addressed to talk to perform subsequent reads. EDR (R1) may also be used to capture data in this format.

Example:

```
OUTPUT 718;"F3X"          select decimal mode
ENTER 718; A$             read data from the Digital I/O Interface
DISP A$                   display shows 240;165
OUTPUT 718;D100;200ZX     output 100 & 200 to the Digital I/O Interface
ENTER 718; A$             read data from the Digital I/O Interface
DISP A$                   display shows 100;200
```

F4 Format—Binary

In the F4 binary format, no error checking is performed. Be careful when using this mode to avoid locking the IEEE bus.

When addressed to listen, the Digital I/O Interface expects the "D" prefix followed by five bytes of data beginning with PORT5 without the "Z" suffix. If any digital I/O port is configured as an input, the data to that input port will be ignored.

When the Digital I/O Interface is addressed to talk (R0), it asserts Inhibit, reads the data from all ports, unasserts Inhibit, and outputs 5 bytes beginning with PORT5 with EOI asserted on the last byte. Bus terminators, with the exception of EOI, are not appended to the output. After output the Digital I/O Interface must be re-addressed to talk to perform subsequent reads. EDR (R1) may also be used to capture data in this format.

F5 Format—High-Speed Binary

In the F5 high-speed binary format, the command interpreter is disabled. When addressed to listen, the Digital I/O Interface treats all bytes received as data to be output to the Digital I/O ports. Each time it receives five bytes or detects EOI asserted, it pulses the Data Strobe for approximately 15 microseconds. Data is expected in the sequence PORT5, PORT4, PORT3, PORT2, PORT1. If only two bytes are received, with EOI asserted on the second byte, the Digital I/O Interface will update PORT5 with the first byte received, PORT4 with the second and pulse

the Data Strobe. Since the interface treats all received characters as data, the Un command will not be recognized.

To place the Digital I/O Interface in the F5 format, the 3 character string "F5X" should be the last command sent to the interface without terminators. Any characters appended to this command, such as carriage return or line feed, will be considered data and the output ports will reflect those character values.

When the Digital I/O Interface is addressed to talk in this format it asserts Inhibit, reads the data from all ports, unasserts Inhibit and outputs the binary data to the bus with EOI asserted on the fifth byte. When the last data byte is transferred, the data is read again in anticipation of another data transfer. If Inhibit is used to sequence external hardware, this line will pulse N+l times; where N is the number of total (5-byte) data transfers. In this format the Digital I/O Interface does not have to be re-addressed to talk to read the ports multiple times. EDR cannot be used to capture data in the F5 high-speed binary format.

The only programmable method to exit the F5 high-speed binary format is device clear (DCL) or Selected Device Clear (SDC). When received, it enables the command interpreter and changes the format to F0. All other parameters remain unchanged. In addition, the Clear output line is not pulsed by DCL or SDC when the interface is in F5.

4.11 Handshake (Hn)

The Handshake control command enables software control of the handshake lines, independent of any other I/O operations. When the Digital I/O Interface receives an Hn command, the respective handshake line is pulsed for approximately 50 microseconds. It returns to its steady-state condition after pulsing. The Invert command may be used to change the active state of any of the handshake lines.

H0 The Clear line is pulsed
H1 The Strobe line is pulsed
H2 The Trigger line is pulsed

Example:

```
OUTPUT 718;"HlX"
```
the Strobe line is pulsed

4.12 Inhibit (Qn)

The Inhibit control command allows software control of the Inhibit line, independent of any other I/O activities. The "set" and "clear" levels of the Inhibit line are determined by the Invert command.

Q0 Clear the Inhibit line (return to unasserted state)
Q1 Set the Inhibit line (place in the asserted state)

Example:

```
CLEAR 718            reset the Digital I/O Interface
OUTPUT 718;"Q1X"     set the Inhibit line
```

4.13 Invert (In)

The Invert command is used to change the polarity of the handshake and data lines. At power-up, all handshake and control lines are active high (logic one = +5 volts). The Invert command can selectively change the polarity of each of the handshake lines, and of the data lines. If multiple Invert commands are contained within the same string, then an Execute command (X) should be included after each Invert command. An alternative is to add the values of each Invert command desired, and send one command with the sum of the desired commands. The Invert commands are ORed together as received. To delete any one command, you must program the default mode 10, then reprogram the desired commands.

10 All control lines are active high, all data lines are high true
11 Inhibit output is active low
12 Trigger output is active low
14 Data Strobe output is active low
18 Clear output is active low
116 Data is low true
132 EDR input is falling-edge sensitive
164 Service input is falling-edge sensitive

Example:

```
CLEAR 718                reset the Digital I/O Interface
OUTPUT 718;"I32XI64X"    select EDR and Service input as falling-edge
                         sensitive
```

NOTE

`OUTPUT 718;"I96X"` performs the same function.

4.14 Port (Pn)

The Port command determines which port is selected for data input/output. In the default mode (P0), all ports are selected. The Pl through P5 commands select a specific eight bit port.

We recommend that you use the Bus Output command with the PO mode to determine which ports will be output when the Digital I/O Interface is addressed to talk. Data in modes Pl through P5 will be input or output in groups of eight bits.

P0 All five ports are selected
Pl Port 1 is selected
P2 Port 2 is selected
P3 Port 3 is selected
P4 Port 4 is selected
P5 Port 5 is selected

Example:

```
CLEAR 718            reset the Digital I/O Interface
OUTPUT 718;"P4X"     select port 4
```

4.15 Service Request Mask (SRQ) Mn

The Service Request (SRQ) mode is used by the Digital I/O Interface to alert the controller to one of several conditions described below. Multiple SRQ conditions can be enabled simultaneously by issuing them separately or by combining them in one command. If multiple SRQ commands are contained within the same command string, each SRQ command should be followed by an Execute command (X). The programmed SRQ modes will remain enabled until the M0 command is sent, or the controller sends a Device Clear (DCL), Selected Device Clear (SDC), or Interface Clear (IFC) command.

M0 SRQ is disabled
M1 SRQ on Service input transition
M2 SRQ on EDR input transition
M4 SRQ on bus error

M8 SRQ on Self-Test error
Ml6 SRQ on Ready

M0 default mode disables the SRQ function, preventing the Digital I/O Interface from generating a Service Request.

Ml will generate a Service Request when the Service Input line makes a transition. Refer to the Invert command (I64) description for programming the polarity of the Service input line.

M2 will generate a Service Request when the EDR input makes a transition.

Refer to the Invert command (I32) description for programming the polarity of the EDR input line.

M4 will generate a Service Request when a bus error occurs. The most common bus error is sending an invalid command to the Digital I/O Interface. For example, attempting to select an "F6" format when no "F6" format exists will generate a Service Request when the M4 mode is selected.

M8 will generate a Service Request when the self-test fails. Refer to the Test command (T0) description for details on self-tests.

M16 will generate a Service Request when the Digital I/O Interface has completed the execution of a set of commands from the bus controller. This is used by the controller to assure the completion of a set of commands before sending a subsequent set of commands.

Example:

```
CLEAR 718              reset the Digital I/O Interface
OUTPUT 718;"M4X"       select SRQ on Bus error
OUTPUT 718;"F7X"       send an invalid bus command
```

NOTE

Error and SRQ LEDs should light.

```
CLEAR 718              reset the Digital I/O Interface
OUTPUT 718;"M1XM4X"    select SRQ on Bus error and SRQ on Service input
OUTPUT 718;"M5X"       This has the same effect as the command above where
                       M1X plus M4X equals M5X.
```

4.16 Serial-Poll Status Byte

The Interface sends the Serial Poll Output byte when it receives the serial poll command from the controller. Refer to the SRQ description for details on how the Serial Poll byte is affected. Below is a description of the significance of each bit in the Serial Poll byte.

Bit Location	Significance (SRQ Bit Value if set to logic 1)	
DIO1 (LSB)	1	Service Input transition
DIO2	2	EDR input transition
DIO3	4	Bus error
DIO4	8	Test error
DIO5	16	Ready for more commands
DIO6	32	Not assigned, always 0
DIO7	64	Service Request bit
DIO8 (MSB)	128	Not assigned, always 0

Serial Poll Bit Description

- DIO1: When enabled by the M1 command, DIO1 is set by a transition on the Service Input line (active transition state determined by the Invert command [164]). DIO1 is cleared after the controller serial polls the Digital I/O Interface.
- DIO2: When enabled by the M2 command, DIO2 is set on an EDR transition (active transition state determined by the Invert command [132]). DIO2 is cleared after the controller serial polls the Digital I/O Interface.
- DIO3: DIO3 is set when an invalid command is sent to the Digital I/O Interface. The M4 command will enable a Service Request to occur, then an invalid command is received. The bit is cleared after the controller sends a Status command (UOX) and reads the status string from the Digital I/O Interface.
- DIO4: The status of DIO4 is determined after the Test command (TOX) is sent to the Digital I/O Interface. If the self-test passes, the DIO4 bit will remain a zero. If the self test fails, DIO4 will be set to a logic 1. The M8 command will cause a Service Request to be generated in addition to DIO4 being set if the self-test fails. The DIO4 bit is cleared after the controller sends a Status command (UOX) and reads the status string from the Digital I/O Interface.

- DIO5: The DIO5 bit is set after an entire command string has been received and processed by the Digital I/O Interface. The bit is clear while the Digital I/O Interface is processing commands that have been received from the controller. When used with the M16 command, a Service Request will also be generated when the DI05 bit is set. An Execute command (X) must be received before the DI05 bit can be cleared.

- DIO6: DIO6 is not used, and is always a logic zero.

- DIO7: When the Digital I/O Interface generates a Service Request, the DIO7 will be set to a logic one. This is used by the controller to determine that the Service Request was generated by the Digital I/O Interface.

- DIO8: DIO8 is not used, and is always a logic zero.

Example:

```
CLEAR 718              reset the Digital I/O Interface
OUTPUT 718;"M4X"       select SRQ on Bus error
OUTPUT 718;"F7X"       send an invalid bus command. ERROR and SRQ LEDs
                       should light.
SPOLL (718)            display should be 84 (64+16+4)
```

64 means the Digital I/O Interface was the source of the SRQ. 16 means the Digital I/O Interface is READY for more commands. 4 denotes a Bus error.

When serial polled, the SRQ LED will turn off.

4.17 Status (Un)

The Status command (U0) will cause the Digital I/O Interface to send the status message when next addressed to talk. The status of the Digital I/O Interface may be read at any time without interfering with normal operation. Any error conditions are cleared after the status string is read by the controller. The Status command (Un) also enables the controller to read any single bit from the I/O ports (U1 through U40).

U0 Send the Digital I/O Interface status when next addressed to talk
Un Send the status of bit n (1 through 40) when next addressed to talk

The format of the status byte returned by the Digital I/O Interface after receiving a U0 command is as follows:

*.*C#E#F#G#I###K#M###P#R#Y#

where each # equals the number corresponding to that command. The leading information *.* is the revision level of the Digital I/O Interface firmware.

Example:

```
DIM A$[50]          dimension A$
CLEAR 718           reset the Digital I/O Interface
OUTPUT 718;"UOX"    send U0 to the Digital I/O Interface
ENTER 718; A$               read the status-byte display
DISP A$             1.0C0E0F0G0I000K0M000P0R0Y0
```

The status returned after receiving a U1 through U40 is an ASCII character "1" or "0," depending on the level of the line, and the state of the Invert command (I16).

```
CLEAR 718           reset the Digital I/O Interface
OUTPUT 718;"U22X"   request the status of bit 22
ENTER 718;A$        read the status bit
DISP A$             display shows a 0 (dependent on the signal applied to
                    the input)
```

Below is a summary of the Status (U0) information.

C#	Configuration
C0	All ports are inputs
C1	Port 1 is an output, ports 2 through 5 are inputs
C2	Ports 1 and 2 are outputs, ports 3 through 5 are inputs
C3	Ports 1 through 3 are inputs, ports 4 and 5 are inputs
C4	Ports 1 through 4 are outputs, port 5 is an input
C5	All ports are outputs

E#	Error Message
0	No error
1	Unrecognized command (for example, W3)
2	Illegal command option (for example, F8)
3	Conflict (attempt to output data to an input port)
4	ROM error
5	RAM error

F#	Data Format
F0	Hexadecimal
F1	ASCII
F2	Binary
F3	Decimal
F4	High Speed Binary

I###	Invert Control Lines
I0	All control and data lines are active high
I1	Inhibit output is active low
I2	Trigger output is active low
I4	Data Strobe output is active low
I8	Clear output is active low
I16	Data is active low
I32	EDR input is falling edge sensitive
I64	Service input is falling edge sensitive

NOTE

The status indication reflects the sum of all received Invert commands.

K#	End or Identify
K0	EOI enabled
K1	EOI disabled

M##	Service Request
M0	SRQ is disabled
M1	SRQ on Service input transition
M2	SRQ on EDR input transition
M4	SRQ on Bus error
M8	SRQ on Test error
M16	SRQ on Ready

NOTE

The status indication reflects the sum of all received Service Request commands.

P#	Selected Port
P0	All ports selected
P1	Port 1 selected
P2	Port 2 selected
P3	Port 3 selected
P4	Port 4 selected
P5	Port 5 selected

R#	Data Ready
R0	Data is not latched, but is read when the Digital I/O Interface is addressed to talk
R1	Data is latched on EDR transition

T#	Test LED
T0	Perform RAM and ROM test

Y#	Terminator
Y0	CR LF
Y1	LF CR
Y2	CR only
Y3	LF only

4.18 Terminator (Yn)

The IEEE 488 bus terminator defaults at power-on to the settings on Switch S1. It also may be programmed for any combination of Carriage Return (CR) and Line Feed (LF). The Y0 mode is the most commonly accepted terminator, CR-LF. Y1 reverses the sequence to send LF-CR. Y2 sends CR only and Y3 sends LF only.

Y0	CR LF
Y1	LF CR
Y2	CR only
Y3	LF only

Example:

```
CLEAR 718
OUTPUT 718;"Y3X"     select line-feed terminator
```

4.19 Test (T0)

The Test command is used to verify hardware and LED operation.

T0	Perform RAM and ROM test

The T0 command will cause the Digital I/O Interface to initiate a ROM/RAM test. If the test is successful, all LEDs will flash for one-half second. If a test fails, the

Error LED will remain lit. Use the Status command to determine the cause of the self-test error.

Example:

```
CLEAR 718              reset the Digital I/O Interface
OUTPUT 718;"TOX"       send self-test command
```

5. IEEE 488 Primer

5.1 History

The IEEE 488 bus is an instrumentation communication bus adopted by the Institute of Electrical and Electronic Engineers in 1975 and revised in 1978. The Digital I/O Interface conforms to the most recent revision, designated IEEE 488-1978.

Before adopting this standard, most instrumentation manufacturers offered their own versions of computer interfaces. This placed the burden of system hardware design on the end user. If his application required the products of several different manufacturers, then he might need to design several different hardware and software interfaces. The IEEE 488 interface (sometimes called the General Purpose Interface Bus or GPIB) is popular because it totally specifies the electrical and mechanical interface as well as the data transfer and control protocols. The use of the IEEE 488 standard has moved the responsibility of the user from design of the interface to design of the high level software that is specific to the measurement application.

5.2 General Structure

The main purpose of the GPIB is to transfer information between two or more devices. A device can either be an instrument or a computer. Before any information transfer can take place, you must first specify which will do the talking (send data) and which devices will be allowed to listen (receive data). The decision of who will talk and who will listen usually falls on the System Controller—which is, at power-on, the Active Controller.

The System Controller is similar to a committee chairman. On a well-run committee, only one person may speak at a time and the chairman is responsible for recognizing members and allowing them to have their say. On the bus, the device that is recognized to speak is the Active Talker. There can only be one Talker at a time if the information transferred is to be clearly understood by all. The act of "giving the floor" to that device is called Addressing to Talk. If the committee chairman can not attend the meeting, or if other matters require his attention, he can appoint an acting chairman to take control of the proceedings. For the GPIB, this device becomes the Active Controller.

At a committee meeting, everyone present usually listens. This is not the case with the GPIB. The Active Controller selects which devices will listen and commands all other devices to ignore what is being transmitted. A device is

instructed to listen by being Addressed to Listen. This device is then referred to as an Active Listener. Devices that are to ignore the data message are instructed to Unlisten.

The reason some devices are instructed to Unlisten is quite simple. Suppose a college instructor is presenting the day's lesson. Each student is told to raise their hand if the instructor has exceeded their ability to keep up while taking notes. If a hand is raised, the instructor stops his discussion to allow the slower students the time to catch up. In this way, the instructor is certain that each and every student receives all the information he is trying to present. Since there are a lot of students in the classroom, this exchange of information can be very slow. In fact, the rate of information transfer is no faster than the rate at which the slowest note-taker can keep up. The instructor, though, may have a message for one particular student. The instructor tells the rest of the class to ignore this message (Unlisten) and tells it to that one student at a rate which he can understand. This information transfer can then happen more quickly, because it need not wait for the slowest student.

The GPIB transfers information in a similar way. This method of data transfer is called handshaking. More on this later.

For data transfer on the IEEE 488, the Active Controller must…

a) Unlisten all devices to protect against eavesdroppers.

b) Designate who will talk by addressing a device to talk.

c) Designate all the devices who are to listen by addressing those devices to listen.

d) Indicate to all devices that the data transfer can take place.

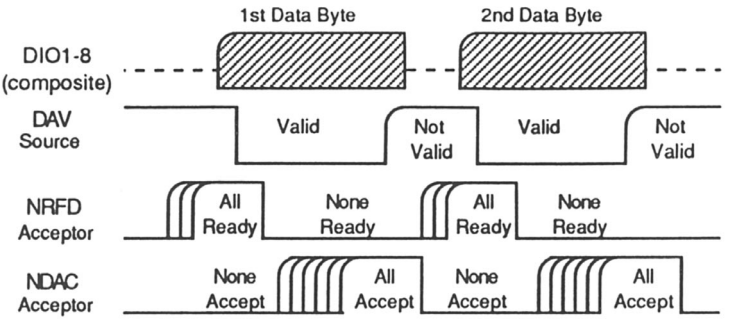


Figure 5-1. IEEE 488 Bus Handshaking.

5.3 Send it to My Address

The IEEE 488 standard permits up to 15 devices to be configured within one system. Each of these devices must have a unique address to avoid confusion. In a similar fashion, every building in town has a unique address to prevent one home from receiving another home's mail. Exactly how each device's address is set is specific to the product's manufacturer. Some are set by DIP switches in hardware, others by software. Consult the manufacturer's instructions to determine how to set the address.

Addresses are sent with universal (multiline) commands from the Active Controller. These commands include My Listen Address (MLA), My Talk Address (MTA), Talk Address Group (TAG), and Listen Address Group (LAG).

5.4 Bus Management Lines

Five hardware lines on the GPIB are used for bus management. Signals on these lines are often referred to as uniline (single-line) commands. The signals are active low; a low voltage represents a logic "1" (asserted), and a high voltage represents a logic "0" (unasserted).

5.4.1 Attention (ATN)

ATN is one of the most important lines for bus management. If Attention is asserted, then the information contained on the data lines is to be interpreted as a multiline command. If it is not, then that information is to be interpreted as data

for the Active Listeners. The Active Controller is the only bus device that has control of this line.

5.4.2 Interface Clear (IFC)

The IFC line is used only by the System Controller. It is used to place all bus devices in a known state. Although device configurations vary, the IFC command usually places the devices in the Talk and Listen Idle states (neither Active Talker nor Active Listener).

5.4.3 Remote Enable (REN)

When the System Controller sends the REN command, bus devices will respond to remote operation. Generally, the REN command should be issued before any bus programming is attempted. Only the System Controller has control of the Remote Enable line.

5.4.4 End or Identify (EOI)

The EOI line is used to signal the last byte of a multibyte data transfer. The device that is sending the data asserts EOI during the transfer of the last data byte. The EOI signal is not always necessary as the end of the data may be indicated by some special character such as carriage return.

The Active Controller also uses EOI to perform a Parallel Poll by simultaneously asserting EOI and ATN.

5.4.5 Service Request (SRQ)

When a device desires the immediate attention of the Active Controller, it asserts SRQ. It is then the Controller's responsibility to determine which device requested service. It does this via a Serial Poll or a Parallel Poll.

5.5 Handshake Lines

The GPIB uses three handshake lines in an "I'm ready—Here's the data—I've got it" sequence. This handshake protocol assures reliable data transfer, at the rate determined by the slowest Listener. One line is controlled by the Talker, while the other two are shared by all Active Listeners. The handshake lines, like the other IEEE 488 lines, are active low.

5.5.1 Data Valid (DAV)

The DAV line is controlled by the Talker. The Talker verifies that NDAC is asserted (active low) which indicates that all Listeners have accepted the previous data byte

transferred. The Talker then outputs data on the bus and waits until NRFD is unasserted (high) which indicates that all Addressed Listeners are ready to accept the information. When NRFD and NDAC are in the proper state, the Talker asserts DAV (active low) to indicate that the data on the bus is valid.

5.5.2 Not Ready for Data (NRFD)

This line is used by the Listeners to inform the Talker when they are ready to accept new data. The Talker must wait for each Listener to unassert this line (high), which they will do at their own rate when they are ready for more data. This assures that all devices that are to accept the information are ready to receive it.

5.5.3 Not Data Accepted (NDAC)

The NDAC line is also controlled by the Listeners. This line indicates to the Talker that each device addressed to listen has accepted the information. Each device releases NDAC (high) at its own rate, but the NDAC will not go high until the slowest Listener has accepted the data byte.

5.6 Data Lines

The GPIB provides eight data lines for a bit parallel/byte serial data transfer. These eight data lines use the convention of DI01 through DI08 instead of the binary designation of W to D7. The data lines are bidirectional and are active low.

5.7 Multiline Commands

Multiline (bus) commands are sent by the Active Controller over the data bus with ATN asserted. These commands include addressing commands for talk, listen, Untalk and Unlisten.

5.7.1 Go To Local (GTL)

This command allows the selected devices to be manually controlled. (IEEE 488 Command Code: $01.)

5.7.2 Listen Address Group (LAG)

There are 31 (0 to 30) listen addresses associated with this group. The 3 most significant bits of the data bus are set to 001 while the 5 least significant bits are the address of the device being told to listen.

5.7.3 UNLISTEN (UNL)

This command tells all bus devices to Unlisten. It's the same as Unaddressed to Listen. (IEEE 488 Command Code: $3F.)

5.7.4 TALK ADDRESS GROUP (TAG)

There are 31 (0 to 30) talk addresses associated with this group. The 3 most significant bits of the data bus are set to 010 while the 5 least significant bits are the address of the device being told to talk.

5.7.5 UNTALK (UNT)

This command tells bus devices to Untalk. It's the same as Unaddressed to Talk. (IEEE 488 Command Code: $5F.)

5.7.6 LOCAL LOCKOUT (LLO)

Issuing the LLO command prevents manual control of the instrument's functions. (IEEE 488 Command Code: $11.)

5.7.7 DEVICE CLEAR (DCL)

This command causes all bus devices to be initialized to a pre-defined or power-up state. (IEEE 488 Command Code: $14.)

5.7.8 SELECTED DEVICE CLEAR (SDC)

This causes a single device to be initialized to a pre-defined or power-up state. (IEEE 488 Command Code: $04.)

5.7.9 SERIAL POLL DISABLE (SPD)

The SPD command disables all devices from sending their Serial Poll status byte. (IEEE 488 Command Code: $19.)

5.7.10 SERIAL POLL ENABLE (SPE)

A device which is Addressed to Talk will output its Serial Poll status byte after SPE is sent and ATN is unasserted. (IEEE 488 Command Code: $18.)

5.7.11 GROUP EXECUTE TRIGGER (GET)

This command usually signals a group of devices to begin executing a triggered action. This allows actions of different devices to begin simultaneously. (IEEE 488 Command Code: $08.)

5.7.12 Take Control (TCT)

This command passes bus control responsibilities from the current Controller to another device that has the ability to control. (IEEE 488 Command Code: $09.)

5.7.13 Secondary Command Group (SCG)

These are any one of the 32 possible commands (0 to 31) in this group. They must immediately follow a talk or listen address. (IEEE 488 Command Codes: $60 to $7F.)

5.7.14 Parallel Poll Configure (PPC)

This configures devices capable of performing a Parallel Poll for which data bit they will assert in response to a Parallel Poll. (IEEE 488 Command Code: $05.)

5.7.15 Parallel Poll Unconfigure (PPU)

This disables all devices from responding to a Parallel Poll. (IEEE 488 Command Code: $15.)

5.8 More About Service Requests

Most of the commands covered, both uniline and multiline, are the responsibility of the Active Controller to send and the bus devices to recognize. Most of these happen routinely by the interface and are totally transparent to the system programmer. Other commands are used directly by the user to provide optimum system control. Of the uniline commands, SRQ is very important to the test system, so the software designer has easy access to this line from most devices. Service Request is the method by which a bus device can signal to the Controller that an event has occurred. It is similar to an interrupt in a microprocessor-based system.

Most intelligent bus peripherals have the ability to assert SRQ. A DMM might assert it when its measurement is complete, if its input is overloaded or for any of an assortment of reasons. A power supply might SRQ if its output has current limited. This is a powerful bus feature that removes the burden from the System Controller to periodically inquire, “Are you done yet?” Instead, the Controller says, “Do what I told you to do and let me know when you’re done” or “Tell me when something is wrong.”

Since SRQ is a single line command, there is no way for the Controller to determine which device requested the service without additional information provided by the multiline commands for Serial Poll and Parallel Poll.

5.8.1 Serial Poll

Suppose the Controller receives a service request. For this example, let's assume there are several devices that could assert SRQ. The Controller issues an SPE (Serial Poll enable) command to each device sequentially. If any device responds with DIO7 asserted it indicates to the Controller that it was the device that asserted SRQ. Often the other bits will indicate why the device wanted service. This Serial Polling sequence, and any resulting action, is under control of the software designer.

5.8.2 Parallel Poll

The Parallel Poll is another way the Controller can determine which device requested service. It provides the who but not necessarily the why. When bus devices are configured for Parallel Poll, they are assigned one bit on the data bus for their response. By using the Status bit, the logic level of the response can be programmed to allow logical OR/AND conditions on one data line by more than one device. When SRQ is asserted, the Controller (under user's software) conducts a Parallel Poll. The Controller must then analyze the eight bits of data received to determine the source of the request. Once the source is determined, a Serial Poll might be used to determine the why.

Of the two polling types, the Serial Poll is the most popular because of its ability to determine the who and why. In addition, most devices support Serial Poll only.

6. Service Information

6.1 Returning the Interface to Black Box

If you encounter problems in using the Digital I/O Interface, call Black Box Technical Support at 724-746-5500. If we can't solve the problem over the phone, we'll give you shipping instructions to return the unit to Black Box.

6.2 Theory of Operation

The heart of the Digital I/O Interface is a 6809 microprocessor (U101) supported by 8K bytes of firmware EPROM (U102 [2764]) and 8K bytes of static RAM (U103 [6264]). A Versatile Interface Adapter (U104 [65B22]) is used to generate real-time interrupts for the firmware operating system. The front-panel annunciators are also driven by U104 through an inverter (U113 [74LS04]).

The IEEE 488 bus interface functions via a TMS9914A (U106) controller with drivers U107 and U108. The digital I/O ports are controlled by "PIA"s (U202-U204 [68B21]). SW1 is read through one port of U204.

Power is supplied by an external unregulated 9 volt wall mount supply. Regulation to the required +5 volts is provided by U109 (7805). Decoding of the microprocessor address space is accomplished with a Programmable Logic Array (U110 [16L8]). The memory space allocation is...

Address	Device	Part Number	Function
$6000-$7FFF	U103	6264	Static RAM
$9200-$9204	U202	6821	Digital I/O
$9400-$9404	U203	6821	Digital I/O
$9800-$9804	U204	6821	Digital I/O
$A000-$A007	U106	TMS	IEEE Controller
$B000-$BOOF	U104	R65C22	VIA
$E000-$FFFF	U102	2764	Programmed EPROM

6.3 Digital I/O Interface Motherboard Component Layout

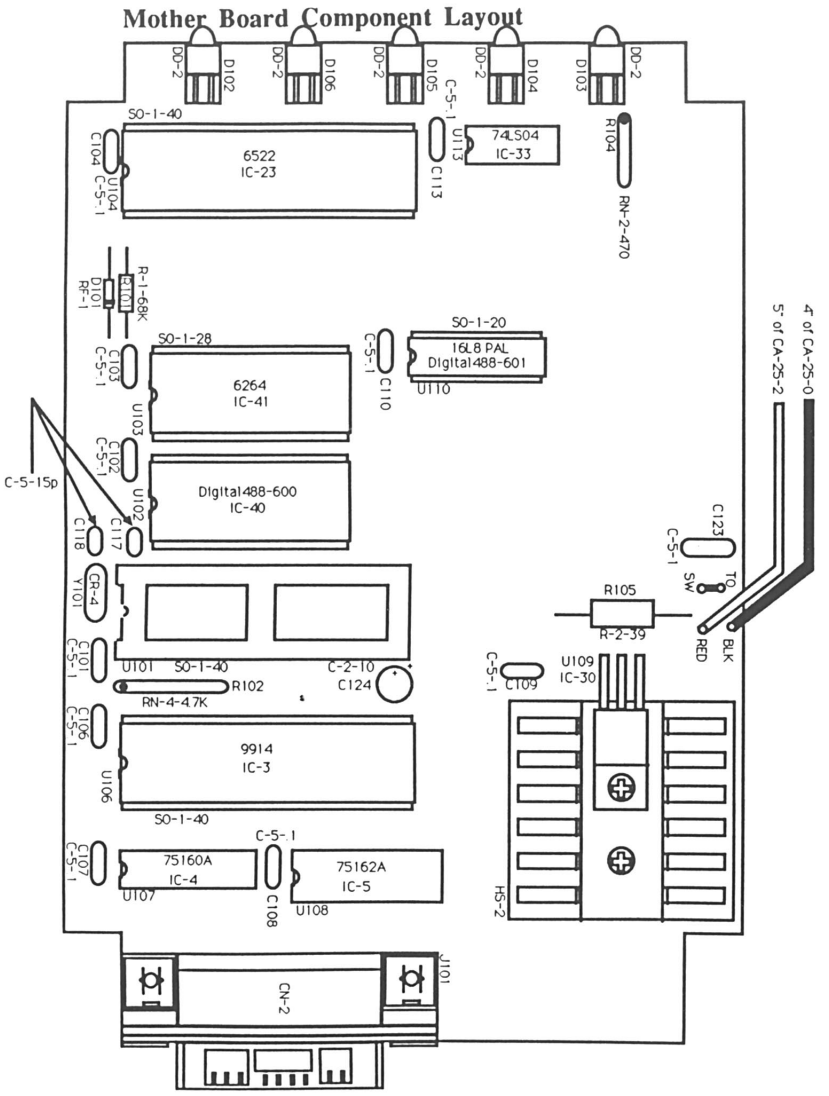


Figure 6-1. Motherboard Layout.

6.4 Digital I/O Interface I/O Board Component Layout

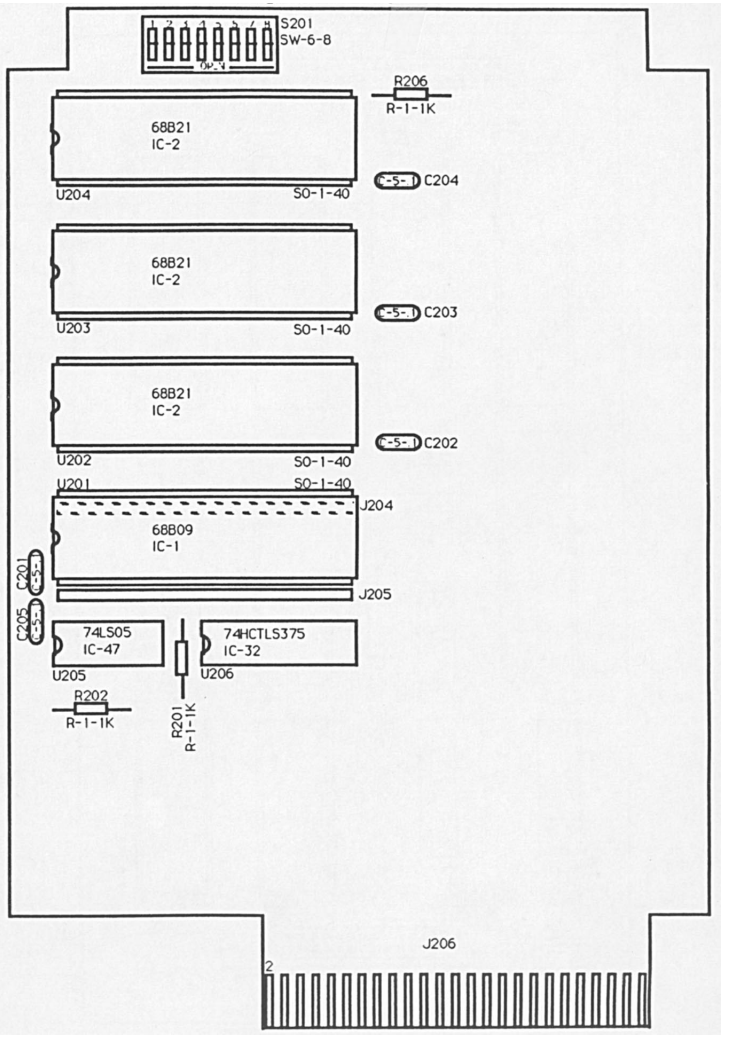


Figure 6-2. I/O Board Layout.

Appendix A: Command Summary

Command	Code	Description
Bit Set	An	Set bit n (1 through 40)
Bit Clear	Bn	Clear bit n (1 through 40)
Bus Output	G0	Input and output port data sent on talk
	G1	Only input port data sent on talk
	G2	Only output port data sent on talk
Configure	C0	All ports are inputs
	C1	Port 1 is an output, ports 2 through 5 are inputs
	C2	Ports 1 and 2 are outputs, ports 3 through 5 are inputs
	C3	Ports 1 through 3 are outputs, ports 4 and 5 are inputs
	C4	Ports 1 through 4 are outputs, port 5 is an input
	C5	All ports are outputs
Data	Dn…Z	Data to be output is entered after “D” and terminated by “Z”
Data Ready	R0	Data is read when system is addressed to talk
	R1	Data is latched on EDR transition
EOI	K0	EOI enabled
	K1	EOI disabled
Execute	X	Execute preceding command string
Format	F0	ASCII Hexadecimal
	F1	ASCII Character
	F2	ASCII Binary
	F3	ASCII Decimal
	F4	Binary
	F5	High-Speed Binary

Command	Code	Description
Handshake	H0	Pulse the clear line
	H1	Pulse the strobe line
	H2	Pulse the trigger line
Inhibit	Q0	Clear inhibit line
	Q1	Set inhibit line
Invert	I0	All control line outputs are active high
	I1	Inhibit output is active low
	I2	Trigger output is active low
	I4	Data strobe output is active low
	I8	Clear output is active low
	I16	Data is low true
	I32	EDR input is falling-edge sensitive
	I64	Service input is falling-edge sensitive
Port	P0	All ports selected
	P1	Port 1 selected
	P2	Port 2 selected
	P3	Port 3 selected
	P4	Port 4 selected
	P5	Port 5 selected
SRQ Mask	M0	SRQ is disabled
	M1	SRQ on service input transition
	M2	SRQ on EDR input transition
	M4	SRQ on bus error
	M8	SRQ on self-test error
	M16	SRQ on ready
Status	U0	Send status information when next addressed to talk (*.*C#E#F#G#I###K#M###P#R#Y#)
	Un	Read state of bit n (1 through 40)

Command	Code	Description
Terminator	Y0	CR LF
	Y1	LF CR
	Y2	CR only
	Y3	LF only
Test	T0	Perform RAM and ROM test

Appendix B: Mechanical Diagrams

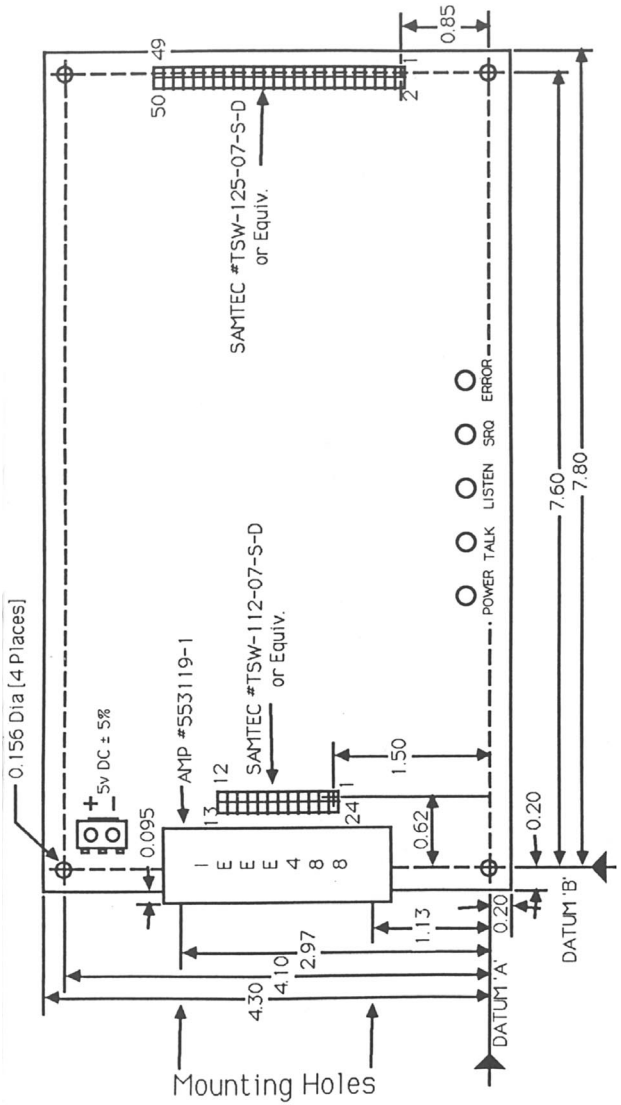
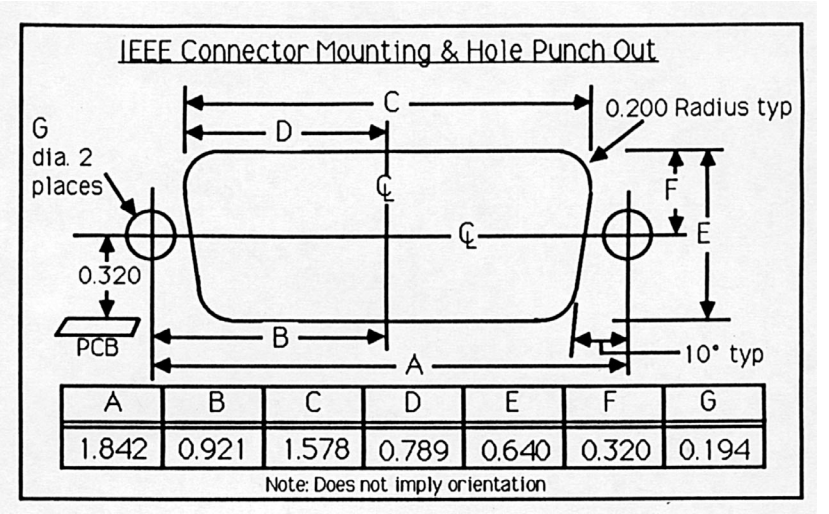


Figure B-1. Board Layout.



A	B	C	D	E	F	G
1.842	0.921	1.578	0.789	0.640	0.320	0.194

Figure B-2. IEEE Connector.

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