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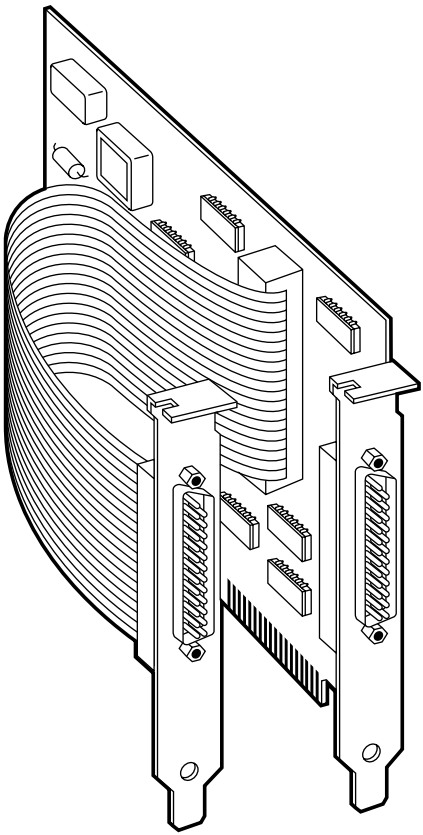
JANUARY 1998
IC120C-R4

RS-530 Dual-Channel High-Speed Sync/Async Adapter



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This equipment generates, uses, and can radiate radio-frequency energy, and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio communication. It has been tested and found to comply with the limits for a Class A computing device in accordance with the specifications in Subpart B of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference when the equipment is operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user at his own expense will be required to take whatever measures may be necessary to correct the interference.

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Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la classe A prescrites dans le Règlement sur le brouillage radioélectrique publié par Industrie Canada.

NORMAS OFICIALES MEXICANAS (NOM)
ELECTRICAL SAFETY STATEMENT

INSTRUCCIONES DE SEGURIDAD

1. Todas las instrucciones de seguridad y operación deberán ser leídas antes de que el aparato eléctrico sea operado.
2. Las instrucciones de seguridad y operación deberán ser guardadas para referencia futura.
3. Todas las advertencias en el aparato eléctrico y en sus instrucciones de operación deben ser respetadas.
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5. El aparato eléctrico no deberá ser usado cerca del agua—por ejemplo, cerca de la tina de baño, lavabo, sótano mojado o cerca de una alberca, etc..
6. El aparato eléctrico debe ser usado únicamente con carritos o pedestales que sean recomendados por el fabricante.
7. El aparato eléctrico debe ser montado a la pared o al techo sólo como sea recomendado por el fabricante.
8. Servicio—El usuario no debe intentar dar servicio al equipo eléctrico más allá a lo descrito en las instrucciones de operación. Todo otro servicio deberá ser referido a personal de servicio calificado.
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10. El equipo eléctrico deber ser situado fuera del alcance de fuentes de calor como radiadores, registros de calor, estufas u otros aparatos (incluyendo amplificadores) que producen calor.
11. El aparato eléctrico deberá ser connectado a una fuente de poder sólo del tipo descrito en el instructivo de operación, o como se indique en el aparato.

12. Precaución debe ser tomada de tal manera que la tierra fisica y la polarización del equipo no sea eliminada.

13. Los cables de la fuente de poder deben ser guiados de tal manera que no sean pisados ni pellizcados por objetos colocados sobre o contra ellos, poniendo particular atención a los contactos y receptáculos donde salen del aparato.

14. El equipo eléctrico debe ser limpiado únicamente de acuerdo a las recomendaciones del fabricante.

15. En caso de existir, una antena externa deberá ser localizada lejos de las lineas de energia.

16. El cable de corriente deberá ser desconectado del cuando el equipo no sea usado por un largo periodo de tiempo.

17. Cuidado debe ser tomado de tal manera que objectos liquidos no sean derramados sobre la cubierta u orificios de ventilación.

18. Servicio por personal calificado deberá ser provisto cuando:

    A: El cable de poder o el contacto ha sido dañado; u

    B: Objectos han caído o líquido ha sido derramado dentro del aparato; o

    C: El aparato ha sido expuesto a la lluvia; o

    D: El aparato parece no operar normalmente o muestra un cambio en su desempeño; o

    E: El aparato ha sido tirado o su cubierta ha sido dañada.

Products bearing the CE Label fulfill the requirements of the EMC directive (89/336/EEC) and of the low-voltage directive (73/23/EEC) issued by the European Commission. To obey these directives, the following European standards must be met:

- EN55022 Class A: "Limits and methods of measurement of radio interference characteristics of information technology equipment"
- EN50082-1: "Electromagnetic compatibility - Generic immunity standard: Part 1: Residential, commercial and light industry"
- EN60950 (IEC950): "Safety of information technology equipment, including electrical business equipment"

CAUTION

This is a Class A Product. In a domestic environment, this product may cause radio interference, and the user may be required to take adequate measures.

Always use cabling provided with this product if possible. If no cable is provided or if an alternate cable is required, use high-quality shielded cabling to maintain compliance with FCC and EMC directives.

CE

Contents

Chapter **Page**

1. Specifications

System Hardware Required — IBM PC compatible computer with one available internal ISA or EISA slot and two available external (bay) slots

Bus Used — ISA

Port Used — None

Interrupt Used — 2 (PC/XT) or 9 (PC/AT), 3, 4, 5, 7, 10, 11, 12, or 15 (user-selectable)

I/O Address Used — Any 8-bit address from 100-107 hex to 3F8-3FF hex (user-selectable)

DMA Channel(s) Used — Many DMA options are available; see **Sections 3.4** and **3.5**

Compliance — CE; FCC Class A, IC Class/classe A

Interface — TIA RS-530; compatible with TIA RS-422 and RS-485; can also support TIA RS-449 with special adapter cable (not included)

Protocol — Synchronous or asynchronous (user-selectable)

Clock Source — Internal or external (from connected device)

Data Format — User-selectable through software

Flow Control — Hardware (RTS, CTS, DSR, DTR), user-programmable; X-ON/X-OFF or other software flow control would have to be handled entirely through software

Operation — Point-to-point (RS-530/422/449) or multipoint (RS-485), user-selectable

Data Rate — Up to 1 Mbps (might be higher depending on the application); user-selectable through software

Maximum Distance — 4000 ft. (1219.2 m) to (farthest) connected device at 100 kbps; at higher speeds, max. distance falls in inverse proportion to data rate, down to 400 ft. (121.9 m) at 1 Mbps

Processor — Zilog 85230 Enhanced Serial Communications Controller (ESSC)

User Controls — (1) 8-position DIP switch for I/O address;
(8) Jumper blocks, with various numbers of positions, for various functions

Diagnostics — SSDACB.EXE diagnostic program on included diskette; Adapter can also be user-programmed to trigger remote digital and local analog loopbacks through connected device

Connectors — (2) DB25 male;
(1) Standard ISA card-edge male

Leads/Signals Supported — See **Appendix A**

Power — +5 VDC at 900 mA from PC's ISA bus

MTBF — Greater than 150,000 hours (calculated)

Temperature Tolerance — Operating: 32 to 122˚F (0 to 50˚C);
Storage: –4 to +158˚F (–20 to +70˚C)

Humidity Tolerance — 10 to 90% noncondensing

Size — Three-quarter-card;
Including card-edge contacts ("goldfingers"):
4.2"H x 5.8"D (10.7 x 14.7 cm);
Excluding card-edge contacts ("goldfingers"):
3.9"H x 5.8"D (9.9 x 14.7 cm)

Weight — 1 lb. (0.5 kg)

2. Introduction

Once you install it in an IBM PC compatible computer, the RS-530 Dual-Channel High-Speed Sync/Async Adapter functions as a pair of high-speed RS-530/422/485 ports capable of either synchronous or asynchronous communication. The Adapter can be used in a variety of sophisticated communications applications that feature SDLC, HDLC, X.25, bisync, monosync, high-speed async, or almost any similar protocol.

The complete Adapter package includes the Adapter card itself, a cable and connector assembly for the Adapter's channel B, a 3.5" diskette containing Developer's Toolkit software, and this manual. If any of these items are missing or damaged, contact Black Box immediately.

The "brain" of the Adapter is the Zilog® 85230 Enhanced Serial Communications Controller (ESCC). You can program this chip for your desired data rate, data format, interrupt control, and DMA control; refer to the ESCC User's Manual. (You can contact Zilog to get a copy of that manual; also, some portions of it are posted on their Web site, www.zilog.com.)

Here are some of the Adapter's important features:

- Two channels of sync/async communications;
- DMA for data rates greater than 1 million bits per second (bps);
- Selectable port address and IRQ level (2/9, 3, 4, 5, 7, 10 , 11, 12, or 15);
- Selectable DMA channel(s) (0, 1, 2, and/or 3);
- EIA-530/422 interface with full modem control that supports the TD, RD, RTS, CTS, DSR, RLSD (DCD), DTR, TSETC (TXC), RSETC (RXC), LL, RL, TM, and TSETT (EXTC) signals (see **Appendix A**); and
- Jumper options for clock source and transmit-driver enabling.

The ESCC's data rate is programmed under software control. The standard oscillator supplied with the Adapter operates at 7.3728 MHz; this frequency can be divided to yield a variety of possible data rates. (The absolute maximum data rate is 1.8432 Mbps, but the Adapter can't maintain that speed for long. Its maximum sustainable data rate will be between 1 and 1.5 Mbps, depending on your application. The minimum data rate is below 50 bps.) If the standard oscillator can't communicate at the data rate you need, we might be able to provide you with an Adapter containing a different crystal that will; call Black Box for technical support.

The Adapter comes from the factory set to these default settings (see **Chapter 3**):

Base Address: 238
IRQ: 5
Port A DMA: TX/RX 1 (hal-duplex)
Port B DMA: TX/RX 3 (half-duplex)
Clock Source: Internal
Driver: TIA RS-530/422

If these settings are OK, the Adapter is ready to be installed; skip to **Chapter 4**. If you need to change any of these settings, go on to **Chapter 3**; and when you are finished configuring the unit, record your settings here:

Base Address: _____
IRQ: _____
Port A DMA: _____
Port B DMA: _____
Clock Source: _____
Driver: _____

3. Configuration

Before you install the RS-530 Dual-Channel High-Speed Sync/Async Adapter, make sure it is configured for proper, conflict-free operation in your computer. There are several controls on its circuit board that determine which system resources it uses, how it operates, and so on. This chapter describes these controls, how to set them, their possible settings, and the corresponding functions.

3.1 Choosing the Address with SW1 Positions 1 Through 7

The RS-530 Dual-Channel High-Speed Sync/Async Adapter occupies eight consecutive locations in the PC's I/O-address space. Use DIP switch SW1 to choose any 8-bit address from 100 to 3FF hex, but be careful: Some of the possible selections might conflict with existing PC ports and other system resources. Table 3-1 below shows several possible settings that we recommend because they usually do not cause conflicts (see **Section 6.1**, step 6).

Table 3-1. Selecting an Address with DIP Switch SW1

Address	Binary	SW1 Posittion Settings						
	A9----------A0	1	2	3	4	5	6	7
238-23F	1000111XXX	Off	On	On	On	Off	Off	Off
280-287	1010000XXX	Off	On	Off	On	On	On	On
2A0-2A7	1010100XXX	Off	On	Off	On	Off	On	On
2E8-2EF	1011101XXX	Off	On	Off	Off	Off	On	Off
300-307	1100000XXX	Off	Off	On	On	On	On	On
328-32F	1100101XXX	Off	Off	On	On	Off	On	Off
3E8-3EF	1111101XXX	Off	Off	Off	Off	Off	On	Off

Figure 3-1 below shows the correlation between the SW1 setting and the bits that represent the Adapter's address. In the illustration, 300 hex (the "base address" for locations 300 through 307 hex) is selected: 300 hex = "11 0000 0XXX" in binary representation. Note that any switch position set "ON" or "closed" corresponds to a "0" in the address, while any position set "OFF" or "open" corresponds to a "1".

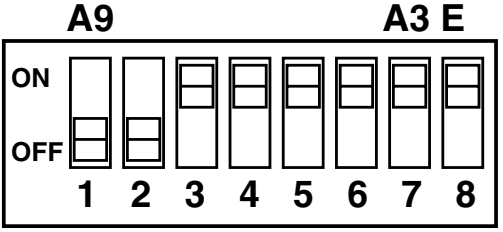


Figure 3-1. DIP Switch SW1.

These are the relative I/O addresses of the Adapter's registers:

- Base address: Channel A Data Port
- Base+1: Channel A Control Port
- Base+2: Channel B Data Port
- Base+3: Channel B Control Port
- Base+4: Board Control/Status Port
- Base+5: Reset TCIRQ

3.2 Deactivating/Reactivating the Adapter with SW1 Position 8

If you ever need to temporarily disable the RS-530 Dual-Channel High-Speed Sync/Async Adapter for any reason, you can deactivate the Adapter by setting position 8 of DIP switch SW1 to "OFF" or "open." You can reactivate the Adapter at any time by setting SW1 position 8 back to "ON" or "closed."

3.3 Setting Clock Source and Driver (RS-485) Options with Jumper Block E8

Use the jumper block labeled E8, shown in Figure 3-2 below, to set two options for the RS-530 Dual-Channel High-Speed Sync/Async Adapter: both the clock source (that is, whether the Adapter gets its clock from its own oscillator or from the connected device) and how the transmit driver is enabled (see the next page). These options can be set independently for each channel: The three jumpers on the block's "A" side apply to channel A (port P1) only, while the three jumpers on the "B" side apply to channel B (port P2) only.

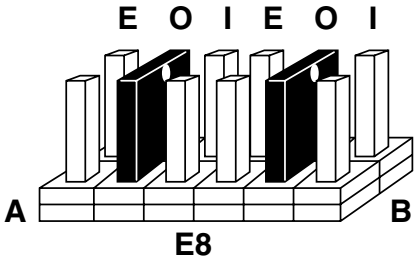


Figure 3-2. Jumper block E8.

- A E *on*: Channel A's transmit driver enabled by RTS (use for RS-485 only)
- A E *removed*: Channel A's transmit driver always enabled
- A O *on*, A I *removed*: Channel A uses internal clock, outputs signal on TSETT
- A O *removed*, A I *on*: Channel A uses external clock from TSETC signal input
- A O and A I *both on* or *both removed*: Invalid setting
- B E *on*: Channel B's transmit driver enabled by RTS (use for RS-485 only)
- B E *removed*: Channel B's transmit driver always enabled
- B O *on*, B I *removed*: Channel B uses internal clock, outputs signal on TSETT
- B O *removed*, B I *on*: Channel B uses external clock from TSETC signal input
- B O and B I *both on* or *both removed*: Invalid setting

In addition to RS-530, the Adapter is capable of RS-422 and RS-485 communication. The settings of block E8's "E" jumpers determine whether the corresponding channel's transmit driver is (a) always enabled or (b) enabled by the Request to Send (RTS) signal from the Adapter's ESCC chip: With the jumper installed (on), RTS enables the driver; with it removed (off), the driver is enabled regardless of the state of RTS. You should install this jumper only if you are using the corresponding Adapter channel in a multipoint polled environment such as RS-485, and only if you have software that knows how to "talk" on the RS-485 bus. *For normal point-to-point RS-530 and RS-422 communication, remove this jumper.*

3.4 Choosing the DMA Channel(s) with Jumper Blocks E4 Through E7

3.4.1 General Information

Use jumper blocks E4 through E7, shown in Figure 3-3 on the next page, to select how each of the RS-530 Dual-Channel High-Speed Sync/Async Adapter's channels handles Direct Memory Access (DMA). Each channel will function in half-duplex or full-duplex DMA mode. Full duplex means that DMA can be used to transmit and receive simultaneously. Half-duplex DMA means that you can either transmit or receive with DMA, but you can't do both simultaneously.

The Adapter's ESCC chip has two signals that correspond to DMA request signals: WAIT/REQ and DTR/REQ. Jumper blocks E5 and E7 control WAIT/REQ and E4 and E6 correspond to DTR/REQ. WAIT/REQ and DTR/REQ can be programmed to serve as DMA request lines (DRQ) by setting the appropriate bits in Write Register 1 and Write Register 14 in the ESCC. WAIT/REQ (E5 & E7) can be programmed for *Transmit* or *Receive* DMA transfers and DTR/REQ (E4 & E6) can be programmed for *Transmit Only*. For additional information on programming the ESCC, please refer to the Zilog ESCC Users Manual (contact Zilog for a copy).

Please note that each DMA channel is selected by two jumpers. Only one DMA channel may be selected for each jumper block. Also refer to **Section 3.5** for DMA-enabling options (software-enabled, always enabled, or never enabled) that can be set with jumper block E2; in particular, if you're not using DMA at all, remove all of the jumpers on E4 through E7 and install a jumper in E2's position "N".

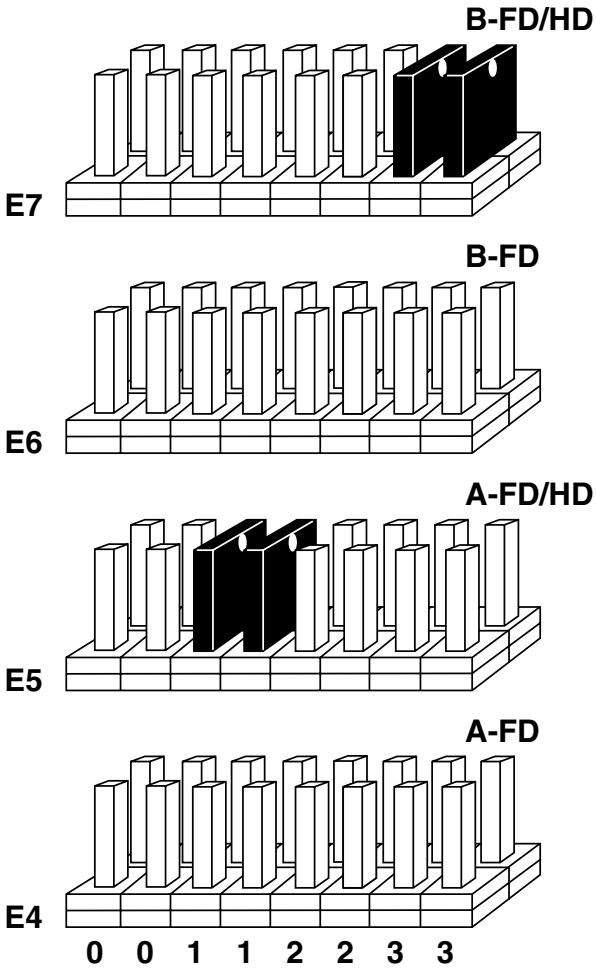


Figure 3-3. Jumper blocks E4 through E7.

Use E4 and E5 to select the DMA channel for the Adapter's channel A (port P1).

Use E6 and E7 to select the DMA channel for the Adapter's channel B (port P2).

3.4.2 Jumper-Option Tables

The tables in this section show how to set jumpers E4 through E7 for each DMA mode.

NOTE

DMA Channel 0 is not available on PC/XT™ class machines, and DMA Channel 2 can only be used if the floppy-disk drive's DMA drivers are turned off. Please refer to the included Toolkit diskette for examples of how to do this with software.

Option	E4	E5	E6	E7
No DMA				
Ch.A No DMA; Ch.B No DMA	None	None	None	None
Single-Channel DMA (Half-Duplex Only)				
Ch. A: DMA ch. 0, half-duplex; Ch. B: No DMA	None	00	None	None
Ch. A: DMA ch. 1, half-duplex; Ch. B: No DMA	None	11	None	None
Ch. A: DMA ch. 2, half-duplex; Ch. B: No DMA	None	22	None	None
Ch. A: DMA ch. 3, half-duplex; Ch. B: No DMA	None	33	None	None
Ch. A: No DMA; Ch. B: DMA ch. 0, half-duplex	None	None	None	00
Ch. A: No DMA; Ch. B: DMA ch. 1, half-duplex	None	None	None	11
Ch. A: No DMA; Ch. B: DMA ch. 2, half-duplex	None	None	None	22
Ch. A: No DMA; Ch. B: DMA ch. 3, half-duplex	None	None	None	33
Double-Channel DMA (Half-Duplex Only)				
Channel A: DMA channel 1, half-duplex; Channel B: DMA channel 3, half-duplex	None	11	None	33
Channel A: DMA channel 0, half-duplex;	None	00	None	22
Single-Channel DMA (Full Duplex)				
Ch. A: DMA ch. 1 receive, ch. 3 transmit; Ch. B: No DMA	33	11	None	None
Ch. A: No DMA; Ch. B: DMA ch. 1 receive, ch. 3 transmit	None	None	33	11
Double-Channel DMA (Full Duplex)				
Ch. A: DMA ch. 1 receive, ch. 3 transmit; Ch. B: DMA ch. 0 receive, ch. 2 transmit	33	11	00	22

3.5 Enabling/Disabling DMA with Jumper Block E2

Use jumper block E2, shown in Figure 3-4 below, to select whether the RS-530 Dual-Channel High-Speed Sync/Async Adapter's DMA tri-state drivers are permanently enabled or disabled or whether the DMA "enable control port" bit is used to enable the DMA hardware request and acknowledge signals. Moving the jumper to position "N" disables the drivers and no DMA can be performed.

NOTES

When you boot the PC, the DMA "software enable" signal will be reset (turned off), so if either channel's jumper is set to "A", you will have to issue the "software enable" signal again.

Please refer to Section 5.1 **for software-bit definitions and examples of DMA driver control.**

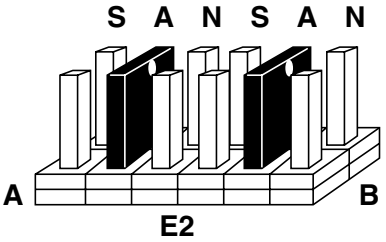


Figure 3-4. Jumper block E2.

A S: DMA is software-enabled on Channel A

A A: DMA is always enabled on Channel A

A N: DMA is never enabled on Channel A

B S: DMA is software-enabled on Channel B

B A: DMA is always enabled on Channel B

B N: DMA is never enabled on Channel B

3.6 Choosing the IRQ with Jumper Block E3

Use jumper block E3, shown in Figure 3-5 below, to select the interrupt request (IRQ) line for the RS-530 Dual-Channel High-Speed Sync/Async Adapter. As shown in the figure below, the jumper posts from left to right correspond to IRQs 2 (for PC/XT machines only—9 for PC/AT® machines), 3, 4, 5, 7, 10, 11, 12, and 15. If you are running the Adapter at low speed in a polling environment and don't want it to use an interrupt, remove the jumper altogether.

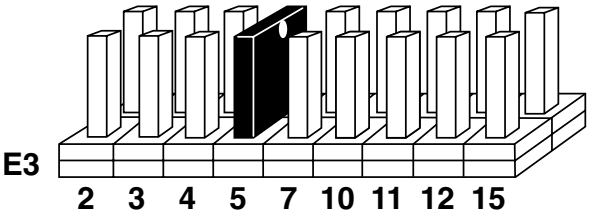


Figure 3-5. Jumper block E3.

3.7 Setting Interrupt Handling with Jumper Block E1

Use jumper block E1, shown in Figure 3-6 below, to select how the RS-530 Dual-Channel High-Speed Sync/Async Adapter handles interrupt requests.

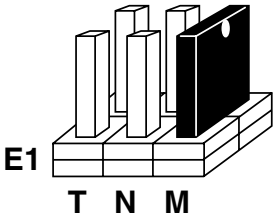


Figure 3-6. Jumper block E1.

In the "N" setting, the Adapter operates in normal, single-interrupt mode.

The "M" setting is for interrupt sharing (that is, multiple cards in the same PC using the same interrupt). It activates a 1-kΩ pull-down resistor required on one port when interrupts are shared by more than one card. If you are sharing one interrupt among two or more Adapters, set one Adapter's E1 block to "M" and remove the E1 jumper altogether on the other Adapter(s). Do *not* set E1 to "M" on *more than one* Adapter in the same PC.

The "T" setting enables the DMA Terminal Count Interrupt. In this setting, the selected DMA channel can generate an interrupt once the DMA Terminal Count has been reached. See **Section 5.2** for more information and refer to the Toolkit diskette for examples of how to handle this through software.

4. Installation

The RS-530 Dual-Channel High-Speed Sync/Async Adapter can be installed in any free ISA or EISA expansion slot in a standard PC. Make sure that the Adapter's configuration controls are set properly for your application (refer to **Chapter 3**).

1. Turn off the PC and unplug its power cord or power supply.
2. Remove the cover of the PC's case.
3. Locate two available external expansion slots in the PC's case and remove their blank metal slot covers.
4. If you will be using the Adapter's channel B (port P2), plug channel B's ribbon cable into the box header labeled E4 on the Adapter. (This cable is keyed to prevent improper installation. If you won't be using channel B, simply set its cable and connector assembly aside.)
5. Gently insert the Adapter itself into an available ISA or EISA slot on the PC's motherboard. Make sure that the Adapter is seated properly.
6. If you are using channel B, attach its connector assembly to the adjacent slot with the retaining screw.
7. Replace the PC case's cover.
8. If you want to run RS-449 from either of the Adapter's ports, you will need to plug an RS-530-to-RS-449 adapter or adapter cable into that port. If you need such a cable, call Black Box for technical support.
9. Run cable (make sure it is the proper type for your chosen interface and application) from the P1 and/or P2 port to the device(s) you want to connect to the Adapter.
10. Plug the PC back in.

This completes your Adapter installation. If it is properly configured, and if you correctly use the proper drivers and software with it, the Adapter should be ready for continuous operation.

5. Operation

5.1 Programming the Adapter

The RS-530 Dual-Channel High-Speed Sync/Async Adapter's controller chip is the Zilog 85230 Enhanced Serial Communications Controller (ESCC). The ESCC's data rate and data format must be programmed through software; see the ESCC Users Manual (contact Zilog for a copy). Programming the modem signals and test signals and turning DMA on or off is somewhat more direct, as explained in the rest of this section.

The Adapter occupies eight Input/Output (I/O) address locations. The ESCC chip uses the first four, while the fifth location (Base+4) is the address of the Adapter's onboard Control/Status Port, which is actually a register. You can use this one-byte register to set the Data Terminal Ready (DTR), Remote Loopback (RL), and Local Loopback (LL) signals, to enable or disable DMA under program control, and to monitor Data Set Ready (DSR) input signals from a connected modem.

Bit	Output Port Bits		Input Port Bits	
0	DTR A	1=On, 0=Off	DSR A	1=Off, 0=On
1	DTR B	1=On, 0=Off	DSR B	1=Off, 0=On
2	LL A	1=On, 0=Off	TM A	1=Off, 0=On
3	RL A	1=On, 0=Off	ESCC INT	1=Off, 0=On
4	LL B	1=On, 0=Off	TM B	1=Off, 0=On
5	RL B	1=On, 0=Off	TC STAT	1=Off, 0=On
6	Ch. B DMA Enable ESCC Ch.B 1=On, 0=Off		Ch.B DMA	1=Off, 0=On
7	Ch. A DMA Enable ESCC Ch.A 1=On, 0=Off		Ch.A DMA	1=Off, 0=On

Here are some examples of pseudocode commands that make use of the Control/Status Port:

Function	Program Bits
Turn On Channel A DTR	Out (Base+4), XXXX XXX1
Turn On Channel B DTR	Out (Base+4), XXXX XX1X
Turn Off Channel A DTR	Out (Base+4), XXXX XXX0
Turn Off Channel B DTR	Out (Base+4), XXXX XX0X
Turn On Channel A LL	Out (Base+4), XXXX X1XX
Turn On Channel B LL	Out (Base+4), XXX1 XXXX
Turn On Channel A RL	Out (Base+4), XXXX 1XXX
Turn On Channel B RL	Out (Base+4), XX1X XXXX
Turn Off Channel A LL	Out (Base+4), XXXX X0XX
Turn Off Channel B RL	Out (Base+4), XX0X XXXX
Enable DMA Drivers	Out (Base+4), 1XXX XXXX
Disable DMA Drivers	Out (Base+4), 0XXX XXXX
Test Channel A DSR	In (Base+4), Mask=0000 0001
Test Channel B DSR	In (Base+4), Mask=0000 0010
Test Channel A TM	In (Base+4), Mask=0000 0100
Test Channel B TM	In (Base+4), Mask=0001 0000

5.2 DMA Terminal Count

The RS-530 Dual-Channel High-Speed Sync/Async Adapter can be set up to operate using a polling method, interrupts, or system DMA. The most efficient method is a combination of DMA and interrupts. The Adapter has been optimized to generate an interrupt at the end of a DMA transfer. This will allow for DMA initialization and buffer management to take place at interrupt time and provide a virtually seamless communication channel. If the "T" option on jumper block E1 is selected (see **Section 3.7**), an onboard latch will be set when Terminal Count for the selected DMA channel(s) is reached. This latch will cause an interrupt to be generated and program execution will be transferred to the application's Interrupt Service Routine (ISR). The DMA Terminal Count Interrupt condition should be reset from the ISR by writing to Base+5. The value that is written to this I/O location is irrelevant. If your application or driver is interrupting on multiple conditions, reading the Status Register located at Base+4 will determine the source of the interrupt (whether it was generated by the ESCC or the DMA Terminal Count). Bit D3 in the Status Port corresponds to a ESCC-generated interrupt and bit D5 corresponds to an interrupt generated by the end of a DMA transfer. Bit D3 can only be reset by polling the ESCC to determine the interrupt source and the action required to reset the interrupt. Please refer to the Software Toolkit and to the 85230 Technical Manual (not included, contact Zilog) for details on, and examples of, programming interrupt and DMA handling.

6. Troubleshooting

6.1 Common Problems

A Developer's Toolkit diskette is supplied with the RS-530 Dual-Channel High-Speed Sync/Async Adapter and can be used for troubleshooting. You can solve most common problems by using this diskette and following these simple steps:

1. Identify all I/O adapters currently installed in your system. This includes your onboard serial ports, controller cards, sound cards, video cards, etc. Find out which I/O addresses and which IRQs (if any) they are using.

2. Configure your Adapter for an address different from that of any other adapter in your system. See **Section 3.1**.

3. Make sure the Adapter is using a unique IRQ. While the Adapter does allow the sharing of IRQs, many other adapters (such as most SCSI adapters and serial ports) do not. The IRQ is typically selected with an onboard jumper block. Refer to the **Section 3.6**.

4. Make sure the Adapter is securely installed in an ISA slot on the motherboard.

5. Use the included diskette to verify that the Adapter is configured correctly. The diskette contains a diagnostic program, "SSDACB.EXE", that will verify whether the Adapter is configured properly. Refer to the "UTIL.TXT" file found in the "\UTIL" subdirectory on the diskette for detailed instructions on using SSDACB.

6. The following are known I/O-address conflicts:
   - 3F8 to 3FF is typically reserved for COM1:
   - 2F8 to 2FF is typically reserved for COM2:
   - 3E8 to 3EF is typically reserved for COM3:
   - 2E8 to 2EF is typically reserved for COM4:. This is a valid setup option for the Adapter; however, because the Adapter only decodes 10 address lines, there might be a conflict with an advanced video card emulating the IBM XGA adapter (8514 register set). This is because such cards sometimes use addresses longer than 10 lines whose first 10 lines hash to something between 2E8 and 2EF.

If you still can't determine the cause of the problem, call Black Box for technical support (see the next section).

6.2 Contacting Black Box

If you determine that the RS-530 Dual-Channel High-Speed Sync/Async Adapter is malfunctioning, *do not attempt to alter or repair the unit.* It has no user-serviceable parts. Call Black Box Technical Support at 724-746-5500.

Before you do, make a record of the history of the problem. We will be able to provide more efficient and accurate assistance if you have a complete description, including:

- the nature and duration of the problem;
- when the problem occurs;
- the components involved in the problem;
- any particular application that, when used, appears to create the problem or make it worse; and
- the results of any testing you've already done.

6.3 Shipping and Packaging

If you need to transport or ship your ServSwitch or ServManager:

- Package it carefully. We recommend that you use the original container.
- If you are shipping the Adapter for repair, make sure you include its channel-B cable and connector assembly. If you are returning the Adapter, make sure you include everything you received with it. Before you ship the unit back to us for any reason, contact Black Box to get a Return Authorization (RA) number.

Appendix A: Pinouts and Termination of the Adapter's Ports

A.1 P1 and P2 Pinouts

Pin #	Abbr.	Name	Direction
1	SHD	Shield	N/A
2	TD A (–)	Transmit Data A	Output
3	RD A (–)	Receive Data A	Input
4	RTS A (–)	Request to Send A	Output
5	CTS A (–)	Clear To Send A	Input
6	DSR A (–)	Data Set Ready A	Input
7	SGND	Signal Ground	N/A
8	RLSD A (–)	Receive Line Signal Detector A*	Input
9	RSETC B (+)	Rcvr. Sgnl. Element Timing (DCE Source) B*	Input
10	RLSD B (+)	Receive Line Signal Detector B*	Input
11	TSETT B (+)	Tmtr. Sgnl. Element Timing (DTE Source) B*	Output
12	TSETC B (+)	Tmtr. Sgnl. Element Timing (DCE Source) B*	Input
13	CTS B (+)	Clear to Send B	Input
14	TD B (+)	Transmit Data B	Output
15	TSETC A (–)	Tmtr. Sgnl. Element Timing (DCE Source) A*	Input
16	RD B (+)	Receive Data B	Input
17	RXC A (–)	Rcvr. Sgnl. Element Timing (DCE Source) A*	Input
18	LL	Local Loopback	Output
19	RTS B (+)	Request to Send B	Output
20	DTR A (–)	Data Terminal Ready A	Output
21	RL	Remote Loopback	Output
22	DSR B (+)	Data Set Ready B	Input
23	DTR B (+)	Data Terminal. Ready B	Output
24	TSETT A (–)	Tmtr. Sgnl. Element Timing (DTE Source) A*	Output
25	TM	Test Mode	Input

*RLSD, RSETC, TSETC, and TSETT are often referred to as DCD (Data Carrier Detect), RXC (Receive Clock), TXC (Transmit Clock), and EXTC or TT (External Clock or Terminal Timing) respectively.

A.2 Line Termination

Typically, each end of a RS-530 or RS-485 bus must have line-terminating resistors, and RS-422 must be terminated on the receive end. On the RS-530 Dual-Channel High-Speed Sync/Async Adapter, a 100-Ω resistor is across each RS-530/422/485 input in addition to a 1-kΩ pull-up/pull-down combination that biases the receiver inputs.

The RS-530 specification calls for a 100-Ω 1/2-watt resistor between the signal ground and the chassis ground. On the IBM PC, these two grounds are already connected together, so the Adapter doesn't carry this resistor.

Appendix B: The Interfaces Explained

B.1 TIA RS-422

The TIA RS-422 specification defines the electrical characteristics of balanced-voltage digital-interface circuits. RS-422 is a differential interface that defines voltage levels and driver/receiver electrical specifications. On a differential interface, logic levels are defined by the difference in voltage between a pair of outputs or inputs. In contrast, a single-ended interface, for example RS-232, defines the logic levels as the difference in voltage between a single signal and a common ground connection. Differential interfaces are typically more immune to the noise and voltage spikes that can occur on communication lines. Differential interfaces also have greater drive capabilities that allow for longer cable lengths. RS-422 is rated up to 10 Megabits per second and can have cabling 4000 feet (1219.2 m) long. RS-422 also defines driver and receiver electrical characteristics that will allow one driver and up to 32 receivers on the line at once. RS-422 signal levels range from 0 to +5 volts. RS-422 does not define a physical connector.

B.2 TIA RS-530

TIA RS-530 (also known as EIA-530 or TIA-530) compatibility means that RS-422 signal levels are met and a certain set of signals is pinned out on a DB25 connector. The Electronics Industries Association (EIA) created the RS-530 specification to detail this pinout, defining a full set of modem-control signals that can be used for regulating flow control and line status. A sister organization, the Telecommunications Industries Association (TIA), is now responsible for maintaining this and related interface specifications. The RS-530 specification defines two types of interface circuits, Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE). The RS-530 Dual-Channel High-Speed Sync/Async Adapter is a DTE interface.

B.3 TIA RS-449

TIA RS-449 (also known as EIA-449 or TIA-449) compatibility means that RS-422 signal levels are met a certain set of signals is pinned out on a DB37 connector. The EIA created the RS-449 specification to detail this pinout, defining a large set of modem-control signals that can be used for regulating flow control and line status.

B.4 TIA RS-485

TIA RS-485 is backward-compatible with RS422; however, it is optimized for party-line or multipoint (multidrop) applications. The output of the RS-422/485 driver is capable of being Active (enabled) or Tri-State (disabled). This capability allows multiple ports to be connected in a multipoint bus and selectively polled. RS-485 allows cable lengths up to 4000 feet (1219.2 m) and data rates up to 10 Megabits per second. The signal levels for RS-485 are the same as those defined for RS-422. RS-485 has electrical characteristics that allow for 32 drivers and 32 receivers to be connected to one line. This interface is ideal for multipoint or network environments. An RS-485 tri-state (not dualstate) driver can remove its own electrical presence from from the line. The driver is in a tri-state or high-impedance condition when this occurs. Only one driver may be active at a time and the other driver(s) must be tri-stated. The output modem-control signal Request to Send (RTS) controls the state of the driver. Some communication software packages refer to RS-485 as “RTS enable” or “RTS block-mode transfer.” RS-485 can be cabled in two ways: two-wire or four-wire. Two-wire mode does not allow for full-duplex communication, and requires that data be transferred in only one direction at a time. For half-duplex operation, the two transmit pins should be connected to the two receive pins (Tx+ to Rx+ and Tx to Rx or Tx– to Rx–). Four-wire mode allows full-duplex data transfers. RS-485 does not define a connector pinout or a set of modem control signals. RS-485 does not define a physical connector.

Appendix C: Direct Memory Access Explained

In many instances it is necessary to transmit and receive data at greater rates than would be possible with simple port I/O. In order to provide a means for trasferring data at higher data rates, a special function called Direct Memory Access (DMA) was built into the original IBM PC. The DMA function allows the RS-530 Dual-Channel High-Speed Sync/Async Adapter (or any other DMA-compatible interface) to read or write data to or from memory without using the PC's microprocessor. This function was originally controlled by the Intel 8237 DMA-controller chip, but may now be a combined function of the peripheral-support chip sets (such as those built by Chips & Technology or Symphony).

During a DMA cycle, the DMA-controller chip is driving the system bus in place of the microprocessor, providing address and control information. When an interface uses DMA, it activates a DMA request signal (DRQ) to the DMA controller, which in turn sends a DMA-hold request to the microprocessor. When the microprocessor receives the hold request it will respond with an acknowledge to the DMA-controller chip. The DMA-controller chip then becomes the owner of the system bus providing the necessary control signals to complete a memory-to-I/O or I/O-to-memory transfer. When the data transfer is started, an acknowledge signal (DACK) is sent by the DMA-controller chip to the Adapter. Once the data has been transferred to or from the Adapter, the DMA controller returns control to the microprocessor.

To use DMA with the Adapter requires a thorough understanding of the PC's DMA functions. The included Developer's Toolkit diskette contains several executables and source-code files that demonstrate how to set up and use DMA. Please refer to the ESCC User's Manual for more information (contact Zilog for a copy).

Appendix D: Asynchronous and Synchronous Communication Explained

Serial data communication implies that individual bits of a character are transmitted consecutively to a receiver that assembles the bits back into a character. Data rate, error checking, handshaking, and character framing (start/stop bits or sync clocking) are predefined; the receiving end must be configured the same way as the transmitting end. The techniques used for serial communication can be divided into two groups, asynchronous and synchronous.

When contrasting asynchronous and synchronous serial communication, the fundamental differences deal with how each method defines the beginning and end of a character or group of characters. The method of determining the duration of each bit in the data stream is also an important difference between asynchronous and synchronous communications. The remainder of this appendix is devoted to detailing the differences between character framing and bit duration implemented in asynchronous and synchronous communication.

D.1 Asynchronous Communication

Asynchronous communication is the standard means of serial data communication for PC/AT and PS/2® compatible computers. The original PC was equipped with a communication or "COM:" port that was designed around an 8250 Universal Asynchronous Receiver Transmitter (UART). This device allows asynchronous serial data to be transferred through a simple and straightforward programming interface. Character boundaries for asynchronous communication are defined by a start bit, followed by a predefined number of data bits (5, 6, 7, or 8), followed by a predefined number of stop bits (1, 1.5 or 2).

An extra bit used for error detection is sometimes included before the stop bit(s). This special bit is called the parity bit. Parity is a simple method of determining if a data bit has been lost or corrupted during transmission. There are several methods for implementing a parity check to guard against data corruption. Common methods are called "even parity" ("E") and "odd parity" ("O"). Usually, however, parity is not used to detect errors on the data stream. This parity option is referred to as "no parity" ("N").

Because each bit in asynchronous communications is sent consecutively, it is easy to generalize asynchronous communication by stating that each character is wrapped (framed) by predefined bits to mark the beginning and end of the serial transmission of the character, as shown in Figure D-1 below. The data rate and communication parameters for asynchronous communication have to be the same at both the transmitting and receiving ends. The communication parameters are data rate, parity, number of data bits per character, and stop bits (as they would be listed, for example, in the argument list for a DOS MODE command: "9600,N,8,1").

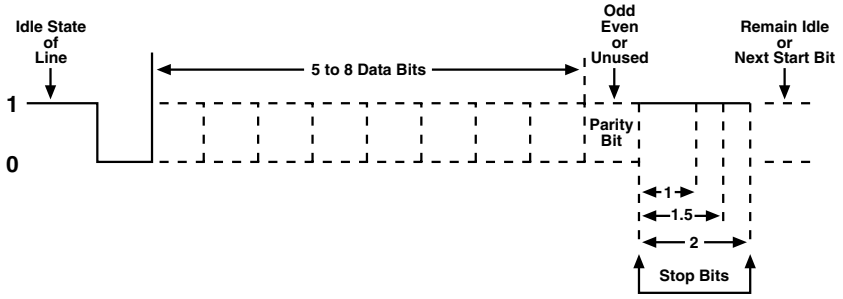


Figure D-1. Asynchronous communication.

D.2 Synchronous Communication

Synchronous communication is used for applications that require higher data rates and more robust error-checking procedures. Character synchronization and bit duration are handled differently from the way they are handled in asynchronous communication. Bit duration in synchronous communication is not necessarily predefined at both the transmitting and receiving ends. Typically, in addition to the data signal, a clock signal is provided. This clock signal will mark the beginning of a bit cell on a predefined transmission. Refer to Figure D-2 on the next page.

The source of the clock is predetermined, and sometimes multiple clock signals are available. For example, if two nodes want to establish synchronous communication, point A could supply a clock to point B that would define all bit boundaries that A transmitted to B. Point B could also supply a clock to point A that would correspond to the data that A received from B. This example demonstrates how communications could take place between two nodes at completely different data rates. Character synchronization in synchronous communication is also very different from the asynchronous method of using start

and stop bits to define the beginning and end of a character. When using synchronous communication, a predefined character or sequence of characters is used to let the receiving end know when to start character assembly.

This predefined character is called a sync character or sync flag. Once the sync flag is received, the communications device will start character assembly. Sync characters are typically transmitted while the communications line is idle or immediately before a block of information is transmitted. To illustrate with an example, let's assume that we are communicating using eight bits per character. Point A is receiving a clock from point B and sampling the receive data pin on every upward clock transition. Once point A receives the predefined bit pattern (sync flag), the next eight bits are assembled into a valid character. The following eight bits are also assembled into a character. This will repeat until another predefined sequence of bits is received (either another sync flag or a bit combination that signals the end of the text, such as the ASCII "EOT" character). The actual sync flag and protocol varies depending on the sync format (SDLC, bisync, etc.).

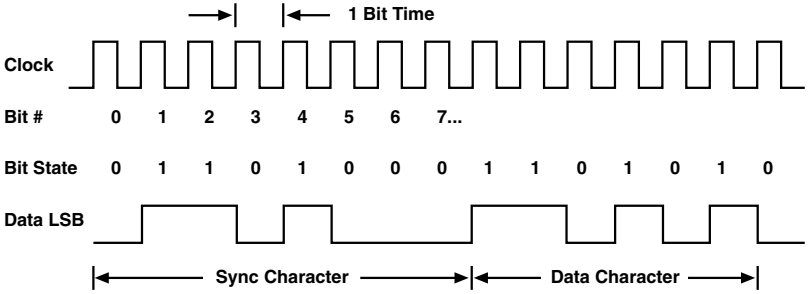


Figure D-2. Synchronous communication.

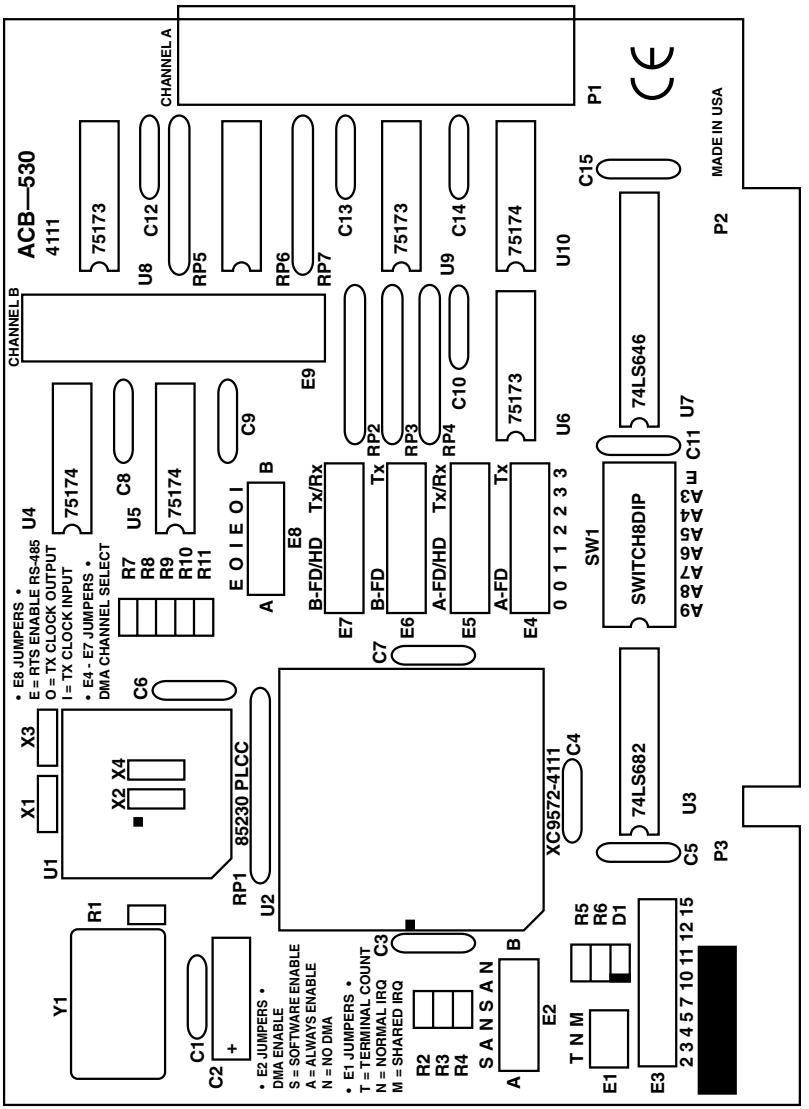
For a more detailed explanation of serial communication, please refer to the book *Technical Aspects of Data Communications* by John E. McNamara.

Appendix E: The Developer's Toolkit Diskette

The Developer's Toolkit diskette included with your RS-530 Dual-Channel High-Speed Sync/Async Adapter provides sample software, a DOS driver, and technical insight to aid in the development of reliable applications for the Adapter. The goal in publishing this collection of source code and technical information is two fold. First, to provide the developer with ample information to develop Adapter-based applications. Second, to provide a channel for suggestions for technical-support efforts.

Free updates to the Developer's Toolkit diskette are available; contact Black Box Technical Support for more information.

Appendix F: The Board Layout



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