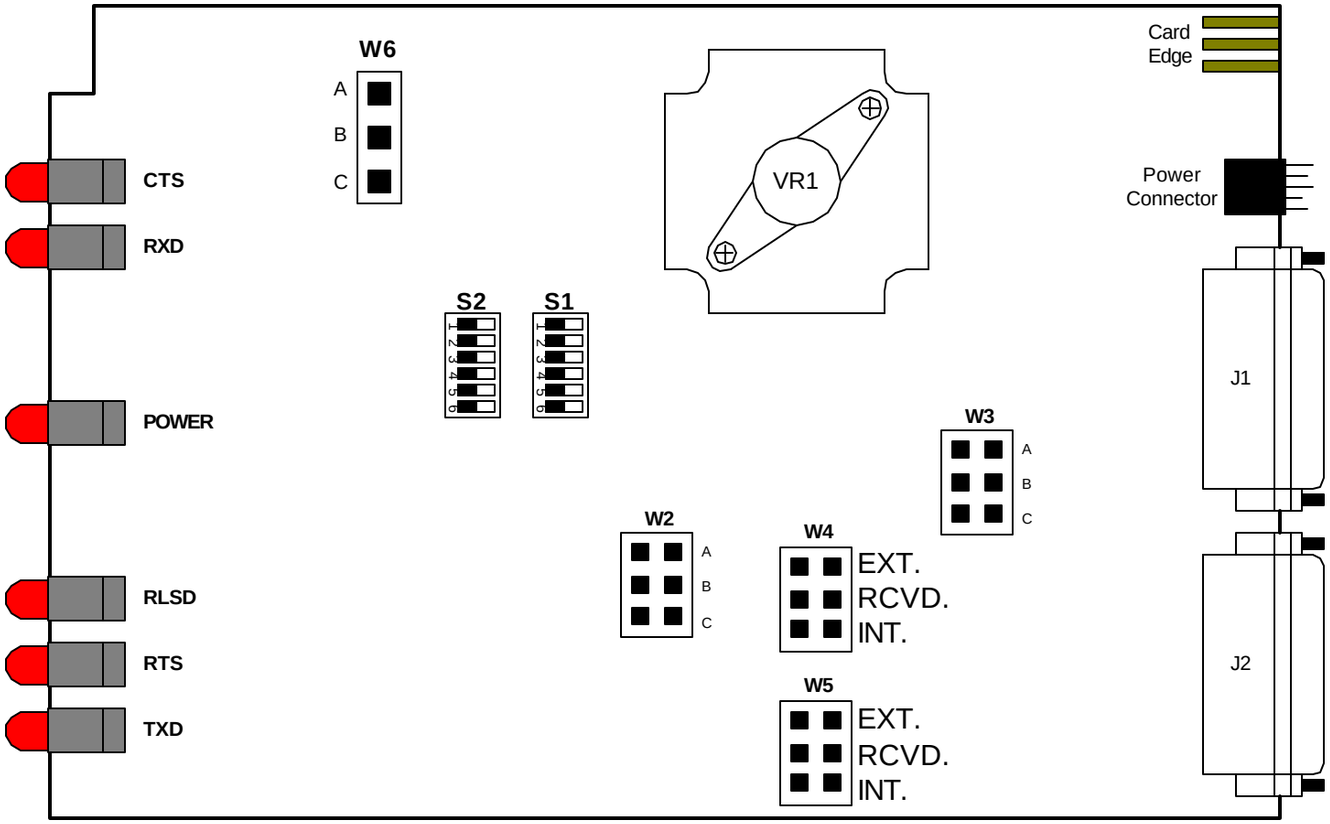

ME108A

DATA RATE:	SWITCH S1 POSITIONS						SWITCH S2 POSITIONS						STRAP W6
	1	2	3	4	5	6	1	2	3	4	5	6	
1,544,000	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	A-B
772,000	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	A-B
2,048,000	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	B-C
1,024,000	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	B-C
512,000	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	B-C
256,000	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF	B-C
128,000	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF	B-C
64,000	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	B-C
32,000	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	ON	ON	ON	ON	B-C

SPECIFICATIONS:

Interface: V.35 Pinned as EIA RS-530

Protocol: Synchronous

Clock Source: Internal or External from either DTE

Operation: Full- or Half-Duplex

Data Rate: Either any speed up to 2.048 Mbps that evenly divides 4.096 Mbps or any speed up to 1.544 Mbps that evenly divides 3.088 Mbps (data-rate regime and individual data rate user-selectable)

Maximum Distance: Up to 2000 ft. on each side, depending on cable quality and data rate.

Connectors: DB25 Female

Power: From wallmount power supply (PS146 for 115VAC; PS146E for 230VAC)
PS146: 115 VAC, 60 HZ at 100 ma; Output = 17VAC CT at 700 ma;
PS146E: 230VAC, 50 HZ at 50 ma; Output = 17VAC CT at 700 ma;

STRAP SETTINGS:

W1: You can use this strap to tie the Frame Ground(V.35 Pin A, RS-530 Pin 1) and Signal Grounds (V.35 Pin B, RS-530 Pins 7 and 23) together. The unit comes from the factory without the grounds tied together.

W2: Determines the Clear-to-Send (CTS) delay on Port J2:
Position A = 50 ms (the factory-default setting)
Position B = 10 ms
Position C = 0 ms

W3: Determines the Clear-to-Send (CTS) delay on Port J1:
Position A = 50 ms (the factory-default setting)
Position B = 10 ms
Position C = 0 ms

W4: Determines the clock source for port J1 (that is, the source of the signals on J1's Serial Clock Transmit pins and J2's Serial Clock Receive pins.
In the EXT. position, timing is external (from J1's Serial Clock Transimit Ext. pins)
In RCVD position, timing is recovered from J2's Serial Clock Transmit Ext. Pins.
In the INT. position, timing is internal (from the units internal clock).

W5: Determines the clock source for port J2 (that is , the source of the signals on J2's Serial Clock Transmit pins and J1's Serial Clock Receive pins.
In the EXT. position, timing is external (from J2's Serial Clock Transmit Ext. pins)
In the RCVD position, timing is recovered from J1's Serial Clock Transmit Ext. pins
Int the INT. position, timing is internal from the units internal clock.

W6: Determines the clock range (that is, which set of data rates the unit can be set for with switches S! and S2)