## ME112A



## Specifications:

## Interface: RS-530

Protocol: Synchronous or Asynchronous
Clock Source: Internal or External from either DTE (user-selectable)
Data Format: Synchronous: 8 data bits; Asynchronous: Transparent to data format
Flow Control: Transparent to software flow control: does not support hardware flow control, but, emulates RTS/CTS delay
Operation: Point-to-Point
Data Rate: Any of 52 user-selectable data rates from 2.4 Kbps to 6.144 Mbps
Maximum Distance: From data or monitor port to attached device: 4000 ft . at data rates up to

Internal Jumpers: (1) 8-position DIP switch for sync/async, clock source, RTS/CTS and RTS/DCD operation, and reclocking enable/disable; (1) Reclock-mode jumper
Indicators: (5) Front-mounted LED's that show the state of SD/TD, RD, CTS, RTS, and DCD on data port J1
Connectors: (2) DB25 Female
Power: Input: 115 VAC at 50 to 60 Hz , consumption 5 watts.

100 Kbps . Above 100 Kbps , drops proportionally as data rate rises, down to 65 ft at 6.144 Mbps

User Controls: (2) "Baud" thumbwheel switches for data rate: (1) "Delay" thumbwheel switch for RTS/CTS delay; and (1) recessed "LB" slide switch to start/stop bidirectional data Baud" thumbwheel switches for data rate: (1) "Delay" thumbwheel sw
RTS/CTS delay; and (1) recessed "LB" slide switch to start/stop bi-

## DIP Switch Settings (SW5)

Position 1 ON: J1; CTS forced High
Position 1 OFF: On data port J1, CTS follows RTS after a delay. (user selectable thru front -panel Delay switch
Position 2 ON: J2; CTS forced High
Position 2 OFF: On data port J2, CTS follows RTS after a delay. (userselectable thru front-panel Delay Switch

Position 3 ON: J1; DCD forced High
Position 3 OFF: J1; DCD follows RTS with no delay
Position 4 ON: J2; DCD forced High
Position 4 OFF: J2; DCD follows RTS with no delay
Position 5 ON: Data reclocking disabled (normal operation)
Position 5 OFF: Data reclocking enabled. Only select this if your equipment inverts the clock polarity. If you select this, you also need to inver he Modem Eliminator's data-reclocking circuitry; do so by moving the internal Reclock Mode jumper (located behind one of the other internal DIP switches, SW3) from posts 1 and 2 (normal, default) to posts 2 and 3 (inverted).

Position 6: is reserved
Positions 7 and 8: Both OFF (default setting): Internal Clock Positions 7 and 8: 7(ON); 8(OFF); External Clock from the DTE on J1 Positions 7 and 8: 7(OFF); 8(ON); External Clock from the DTE on J2 Positions 7 and 8: Both ON; The unit operates ASYNCHRONOUSLY, as must both DTE's (data rate determined by DTE's)

| SWitch <br> Selting | Data <br> Rate | SWitch <br> Setting | Data <br> Rate | SWitch <br> Setting | Data <br> Rate |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 00 | 2.4 K | 17 | 143.36 K | 34 | 768 K |
| 01 | 3.59 K | 18 | 168 K | 35 | 827.08 K |
| 02 | 4.8 K | 19 | 192 K | 36 | 896 K |
| 03 | 7.19 K | 20 | 224 K | 37 | 945.23 K |
| 04 | 9.6 K | 21 | 228.77 K | 38 | 1.024 M |
| 05 | 14.37 K | 22 | 256 K | 39 | 1.07520 M |
| 06 | 16.8 K | 23 | 2799.27 K | 40 | 1.11790 M |
| 07 | 19.2 K | 24 | 336 K | 41 | 1.22880 M |
| 08 | 28 K | 25 | 384 K | 42 | 1.344 M |
| 09 | 28.75 K | 26 | 396.39 K | 43 | 1.53 M |
| 10 | 38.4 K | 27 | 448 K | 44 | 2.048 M |
| 11 | 48 K | 28 | 512 K | 45 | 4.096 M |
| 12 | 56 K | 29 | 555.5 K | 46 | 6.94 M |
| 13 | 64 K | 30 | 565.89 K | 47 | 96 K |
| 14 | 71.86 K | 31 | 614.4 K | 48 | 57.6 K |
| 15 | 112 K | 32 | 672 K | 49 | 14.84 K |
| 16 | 128 K | 33 | 722.82 K | 50 | 3.072 M |

